S21L-7770-03

OEM HARD DISK DRIVE SPECIFICATIONS

for

DJNA-3xxxxx (25.0 GB - 9.1 GB)

3.5-Inch Hard Disk Drive with ATA Interface

Revision (2.0)

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Contents

1.0 General

This document describes the specifications of the following IBM 3.5-inch, ATA interface hard disk drives:

- DJNA-352500 (25.0 GB) (5400 rpm)
- DJNA-352030 (20.3 GB) (5400 rpm)
- DJNA-351520 (15.2 GB) (5400 rpm)
- DJNA-351010 (10.1 GB) (5400 rpm)

- DJNA-372200 (22.0 GB) (7200 rpm)
- DJNA-371800 (18.0 GB) (7200 rpm)
- DJNA-371350 (13.5 GB) (7200 rpm)
- DJNA-370910 (9.1 GB) (7200 rpm)

Note: The specifications in this document are subject to change without notice.

1.1 Glossary

Word	*Meaning*
Kbpi	1 000 Bit Per Inch
Mbps	1 000 000 Bit per second
GB	1 000 000 000 bytes
MB	1 000 000 bytes
KB	1 000 bytes
32 KB	32 x 1 024 bytes
64 KB	64 x 1 024 bytes
Mb/sq.in	1 000 000 bits per square inch
MLC	Machine Level Control
S.M.A.R.T.	Self Monitoring and Analysis Reporting Technology
DFT	Drive Fitness Test

1.2 General Caution

The drive can be easily damaged by shocks or ESD (Electric Static Discharge), so any damages applied to the drive after taking out from shipping package and opening ESD protective bag are user's responsibilities.

2.0 General Features

- Data capacity 25.0 GB - 9.1 GB
- Spindle 7200 / 5400 rpm
- Enhanced IDE (ATA-4)
- Sector format of 512 bytes/sector
- Closed-loop actuator servo (Embedded Sector Servo)
- Dedicated head landing zone
- Automatic Actuator lock
- Interleave factor 1:1
- Read average seek time 8.5 msec excluding command overhead
  Read average seek time 9.0 msec including command overhead
- Sector Buffer 1966 / 430[1] KB
- Ring buffer implementation
- Write Cache
- Queued feature support
- On The Fly correction 12 Bytes
- Automatic Error Recovery procedures for read and write commands
- Self Diagnostics on Power on and resident diagnostics
- Data Trandfer
  - PIO - Mode 4 (16.6 MB/sec)
  - Ultra DMA - Mode 4 (66.6 MB/sec) (Ultra ATA/66)
- CHS and LBA mode
- Transparent Defect Management with ADR (Automatic Defect Reallocation)
- Power Saving modes
- S.M.A.R.T. function support
- Seculity function support
- Default Logical Head Number (16 or 15) selectable with jumper
- Address Offset Feature for DFT implementation

[1] 430KB is only for DJNA-351520/351010.

Part 1. Functional Specification

3.0 Drive Characteristics

This chapter provides the characteristics of the drives.

3.1 Default Logical Drive Parameter

Default of logical drive parameters in Identify Device data are as follows.

Figure 1. Default Drive Parameters

Model	Capacity (GB)	Word 1 (Cyl)	Word 3 (Head)	Word 6 (Sect/Trk)	Word 60-61 (LBA)	Customer Usable Data Bytes
DJNA-352500	25.0	16383	16* 15	63	49,981,680	25,590,620,160
DJNA-352030	20.3	16383	16* 15	63	39,876,480	20,416,757,760
DJNA-351520	15.2	16383	16* 15	63	30,033,360	15,377,080,320
DJNA-351010	10.1	16383	16* 15	63	19,807,200	10,141,286,400
DJNA-372200	22.0	16383	16* 15	63	44,150,400	22,605,004,800
DJNA-371800	18.0	16383	16* 15	63	35,239,680	18,042,716,160
DJNA-371350	13.5	16383	16* 15	63	26,520,480	13,578,485,760
DJNA-370910	9.1	16383	16* 15	63	17,803,440	9,115,361,280

Note:

- The values with * in column of Word 3 (Head) of the above list indicate Ship Default.
- The default value of Word 3 **(Head) can be changed by jumper.**
  For jumper setting, refer to 6.3, “Jumper Settings” on page 45.

3.2 Data Sheet

	DJNA-35xxxx	DJNA-37xxxx
Media Transfer Rate (Mb/sec)	111 - 196	139 - 224
Interface Transfer Rate (MB/sec)	16.6 (PIO Mode-4) 66.6 (Ultra DMA/66)	16.6 (PIO Mode-4) 66.6 (Ultra DMA/66)
Data Buffer Size (KB)	1966 / 430 (note)	1966
Rotational Speed (RPM)	5400	7200
Average Latency (msec)	5.56	4.17
Recording Density (Kbpi)	236 max	220 max
Track Density (TPI)	16,000	15,700
Areal Density (Gb/sq.in.)	3.78 max	3.46 max
Number of Zone	12	12
Number of Data Disks	5/4/3/2	5/4/3/2
Number of Data Heads	10/8/6/4	10/8/6/4
Servo Method	Embeded Sector Servo	Embeded Sector Servo

Figure 2. Mechanical Positioning Performance

Note: 430KB is only for DJNA-351520/351010.

3.3 Performance Characteristics

A file performance is characterized by the following parameters:

- Command Overhead
- Mechanical Positioning
  - Seek Time
  - Latency
- Data Transfer Speed
- Buffering Operation (Look ahead/Write cache)

Note: All the above parameters contribute to file performance. There are other parameters that contribute to the performance of the actual system. This specification tries to define the bare file characteristics, not the system throughput which will depends on the system and the application.

3.3.1 Command Overhead

Command overhead is defined as the time required:

- from the command is written into the command register by a host
- to the assertion of DRQ for the first data byte of a READ command when the requested data is not in the buffer
- exclude
  - Physical seek time
  - Latency time

Command Type (File is in quiescence state)	Time(Typical)	Time(Typical) for Queued command
Read(Cache not hit) (from Command Write to Seek Start)	0.50 msec	0.50 msec
Read(Cache hit) (from Command Write to DRQ)	0.10 msec	0.10 msec
Write (from Command Write to DRQ)	0.015 msec	0.01 msec
Seek (from Command Write to Seek Start)	0.50 msec	Not applicable

Figure 3. Command Overhead

Note: The above table gives an average time.

3.3.2 Mechanical Positioning

3.3.2.1 Average Seek Time (Without Command Overhead, Including Settling)

Command Type	Typical	Max
Read	8.5 msec	9.5 msec
Write	9.5 msec	10.5 msec

Figure 4. Mechanical Positioning Performance

"Typical" and "Max" are given throughout the performance specification by;

Typical Average of the drive population tested at nominal environmental and voltage conditions.

Max Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See section on Environment and D.C. Power Requirement.)

The seek time is measured from the start of motion of the actuator until **a reliable read or write operation may be started**. Reliable read or write implies that error correction/recovery is not employed to correct for arrival problems. The Average Seek Time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{max} (max + 1 - n)\ (Tn.in + Tn.out)}{(max + 1)\ (max)}$$

Where:

- max = Maximum Seek Length
- n = Seek Length (1 to max)
- Tn.in = Inward measured seek time for a n track seek
- Tn.out = Outward measured seek time for a n track seek

3.3.2.2 Full Stroke Seek (Without Command Overhead, Including Settling)

Function	Typical	Max
Read	15.0 msec	18.0 msec
Write	16.0 msec	19.0 msec

Figure 5. Full Stroke Seek Time

Full stroke seek is measured as the average of 1000 full stroke seeks with a **random head switch** from both directions (inward and outward).

3.3.2.3 Head Switch Time (Head Skew)

	DJNA-35xxxx	DJNA-37xxxx
Head Switch Time (Typical)	2.3 msec	1.7 msec

Figure 6. Head Switch Time

A head switch time is defined as the amount of time required by the fixed disk to complete seek the next sequential track after reading the last sector in the current track.

The measurement method is given in 3.3.5, “Throughput” on page 13.

3.3.2.4 Cylinder Switch Time (Cylinder Skew)

	DJNA-35xxxx	DJNA-37xxxx
Cylinder Switch Time (Typical)	3.1 msec	2.3 msec

Figure 7. Cylinder Switch Time

A cylinder switch time is defined as the amount of time required by the fixed disk to complete seek the next sequential block after reading the last track in the current cylinder.

The measurement method is given in 3.3.5, “Throughput” on page 13.

3.3.2.5 Single Track Seek Time (Without Command Overhead, Including Settling)

Function	Typical	Max
Read	1.7 msec	2.4 msec
Write	2.2 msec	2.9 msec

Figure 8. Single Track Seek Time

Single track seek is measured as the average of one (1) single track seek from every track with a **random head switch** in both direction (inward and outward).

3.3.2.6 Average Latency

Model	Time for a revolution	Average Latency
DJNA-35xxxx	11.1 msec	5.56 msec
DJNA-37xxxx	8.3 msec	4.17 msec

Figure 9. Latency Time

3.3.3 Drive Ready Time

	DJNA-35xxxx	DJNA-37xxxx
Power On to Ready	13 sec (typical) / 31 sec (max)	18 sec (typical) / 31 sec (max)

Figure 10. Drive Ready Time

Ready The condition in which the drive is able to perform a media access command (e.g. read, write) immediately.

Power On This includes the time required for the internal self diagnostics.

Note: Max Power On to ready Time is the maximum time period Device 0 waits up to for Device 1 to assert -PDIAG.

3.3.4 Data Transfer Speed

Description	DJNA-35xxxx	DJNA-37xxxx
Disk-Buffer Transfer (Zone 0)		
Instantaneous - typical	19.0 Mbyte/sec	21.8 Mbyte/sec
Sustained - typical	15.5 Mbyte/sec	17.9 Mbyte/sec
Disk-Buffer Transfer (Zone 7)		
Instantaneous - typical	10.9 Mbyte/sec	13.3 Mbyte/sec
Sustained - typical	8.5 Mbyte/sec	10.7 Mbyte/sec
Buffer-Host (max)	66.6 Mbyte/sec	66.6 Mbyte/sec

Figure 11. Data Transfer Speed

- Instantaneous Disk-Buffer Transfer Rate (Mbyte/sec) is derived by:
  (Number of Sectors on a track) * 512 * (Revolution/sec)

  Note: Number of sectors per track will vary because of the linear density recording.

- Sustained Disk-Buffer Transfer Rate (Mbyte/sec) is defined by considering head/cylinder change time. This gives a local average data transfer rate. It is derived by:
  (Sustained Transfer Rate) = A/ (B + C + D)

  A = (Number of Data Sectors per Cylinder) * 512
  B = (# of Surface per cylinder) - 1) * (Head Switch Time)
  C = (Cylinder Change Time)
  D = (# of Surface) * (One Revolution Time)

- Instantaneous Buffer-Host Transfer Rate (Mbyte/sec) defines the maximum data transfer rate on AT Bus. It also depends on the speed of the host.

The measurement method is given in 3.3.5, “Throughput” on page 13.

3.3.5 Throughput

3.3.5.1 Simple Sequential Access

Operation	DJNA-35xxxx typical / max.	DJNA-37xxxx typical / max.
Sequential Read (Zone 0)	1.1 sec / 1.2 sec	1.0 sec / 1.1 sec
Sequential Read (Zone 7)	2.0 sec / 2.1 sec	1.6 sec / 1.7 sec

Figure 12. Simple Sequential Access Performance

The above table gives the time required to read for a total of 8000x consecutive blocks (16,777,216 bytes) accessed by 128 read commands. Typical and Max values are given by 105% and 110% of T respectively throughout following performance description.

Note: Assumes a host system responds instantaneously and host data transfer is faster than sustained data rate.

```
      T = A + B + C + 16,777,216/D + 512/E + DRQ
where:
      T = Calculated Time (sec)
      A = Command Process Time  (Command overhead) (sec)
      B = Average Seek Time (sec)
      C = Average Latency (sec)
      D = Sustained Disk–Buffer Transfer Rate (byte/sec)
      E = Buffer–Host Transfer Rate (byte/sec)
    DRQ = Data ReQuest interval (sec)
```

3.3.5.2 Random Access

Operation	DJNA-35xxxx	DJNA-37xxxx
Random Read (typical / max)	63 sec / 66 sec	58 sec / 60 sec

The above table gives the time required to execute a total of 1000x read commands which access a random LBA.

```
      T = (A + B + C + 512/D + 512/E + DRQ) * 4096

where:
      T = Calculated Time (sec)
      A = Command Process Time  (Command overhead) (sec)
      B = Average Seek Time (sec)
      C = Latency (sec)
      D = Average Sustained Disk–Buffer Transfer Rate (byte/sec)
      E = Buffer–Host Transfer Rate (byte/sec)
    DRQ = Data ReQuest interval (sec)
```

3.3.6 Operating Mode Definition

Operating Mode	Description
Spin-Up	Start up time period from spindle stop or power down.
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Idle	Spindle motor and servo system are working normally. Commands can be received and processed immediately.
Standby	Spindle motor is stopped. Commands can be received immediately, but write or read operations cannot begin until the spindle is spun-up and the Servo system is ready.
Sleep	Spindle motor is stopped. Only soft reset or hard reset can change the mode to standby.

Notes:

1. Upon Power down or Spindle stopped, a head locking mechanism will secure the heads in the ID parking position.

3.3.6.1 Mode Transition Time

From	To	DJNA-37xxxx	DJNA-35xxxx
Standby	Idle	18 sec (typical) / 31 sec (max)	13 (typical) / 31 (max)
Idle	Standby	Immediately	Immediately
Standby	Sleep	Immediately	Immediately
Sleep	Standby	Immediately	Immediately

Figure 13. Mode Transition Time

Note: The actual spin down time will exist, however the command will be processed immediately.

4.0 Data Integrity

4.1 Data loss at Power Off

- The drive retains recorded data under all non-write operation.
- No more than one sector can be lost by power down during write operation while write cache is disabled.
- Power off during write operation may make an incomplete sector which will report hard data error when read. The sector can be recovered by a re-write operation.
- Hard reset does not cause any data loss.

4.2 Write Cache

- Power off while write cache is enabled may cause loss of data which are remaining in the cache and have not been flushed onto the disk media.
  This means that there is a possibility that power off even after write command completion may cause loss of data.
- There are three ways to check if all data in the write cache have been flushed onto the disk. Checking just before power off is recommended to prevent data loss.
  - To confirm successful completion of Software Reset.
  - To confirm successful completion of Flush Cache command.
  - To confirm successful completion of Check Power Mode command.

4.3 Equipment Status

Equipment status is available to the host system any time the drive is not ready to read, write, or seek. This status normally exists at power-on time and will be maintained until the following conditions are satisfied:

- Access recalibration/tuning is complete.
- Spindle speed meets requirements for reliable operation.
- Self-check of drive is complete.

Appropriate error status is made available to the host system if any of the following conditions occur after the drive has once become ready:

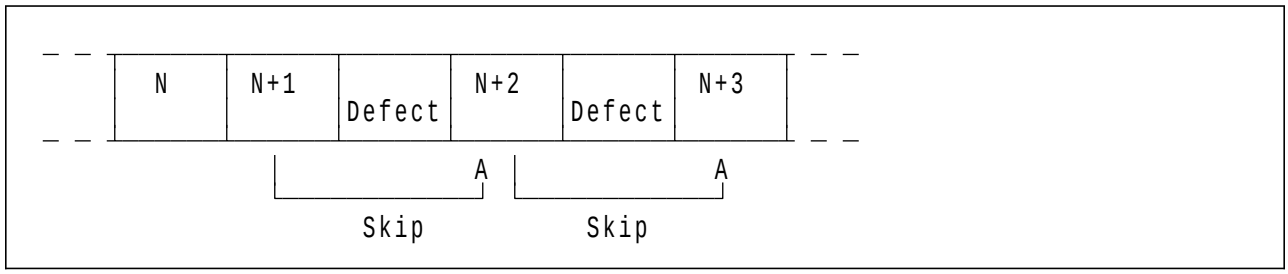
- Spindle speed outside requirements for reliable operation.
- Occurrence of a WRITE FAULT condition.

5.0 Physical Format

Media defects are remapped to the next available sector during Format Process in manufacturing. The mapping from LBA to the physical locations is calculated by an internal maintained table.

5.1 Shipped Format

- Data areas are optimally used.
- No extra sector is wasted as a spare throughout user data areas.
- All pushes generated by defects are absorbed by spare tracks of inner zone.



Defects are skipped without any constraint, such as track or cylinder boundary. The calculation from LBA to physical is done automatically by internal table.

Note: There is possibility to reallocate sectors during drive usage including early period. It is mainly caused by handling problem, and the reallocation is normal maintenance work of Hard Disk Drive.

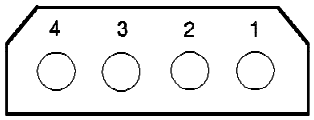
6.0 Specification

6.1 Electrical interface specification

6.1.1 Connectors

6.1.1.1 Power

The DC power connector is designed to mate with AMP (part 1-480424-0) using AMP pins (part 350078-4) strip or (part 61173-4) loose piece, or their equivalents. Pin assignments are shown below.



Pin	Voltage
1	+ 12 V
2	GND
3	GND
4	+ 5 V

Figure 14. Power Connector Pin Assignments

6.1.1.2 AT Signal Connector

The AT signal connector is a 40-pin connector.

6.1.2 Signal Definition

The pin assignments of interface signals are listed as follows:

PIN	SIGNAL	I/O	Type	PIN	SIGNAL	I/O	Type
01	–RESET	I	TTL	02	GND		
03	DD07	I/O	3–state	04	DD08	I/O	3–state
05	DD06	I/O	3–state	06	DD09	I/O	3–state
07	DD05	I/O	3–state	08	DD10	I/O	3–state
09	DD04	I/O	3–state	10	DD11	I/O	3–state
11	DD03	I/O	3–state	12	DD12	I/O	3–state
13	DD02	I/O	3–state	14	DD13	I/O	3–state
15	DD01	I/O	3–state	16	DD14	I/O	3–state
17	DD00	I/O	3–state	18	DD15	I/O	3–state
19	GND			(20)	Key		
21	DMARQ	O	3–state	22	GND		
23	–DIOW(*)	I	TTL	24	GND		
25	–DIOR(*)	I	TTL	26	GND		
27	IORDY(*)	O	3–state	28	CSEL	I	TTL
29	–DMACK	I	TTL	30	GND		
31	INTRQ	O	3–state	32	–HIOCS16	O	OC
33	DA01	I	TTL	34	–PDIAG / –CBLID	I/O	OC
35	DA00	I	TTL	36	DA02	I	TTL
37	–CS0	I	TTL	38	–CS1	I	TTL
39	–DASP	I/O	OC	40	GND		

Figure 15. Table of signals

Notes:

1. "O" designates an output from the Drive.
2. "I" designates an input to the Drive.
3. "I/O" designates an input/output common.
4. "OC" designates Open-Collector or Open-Drain output.
5. The signal lines marked with (*) are redefined during the Ultra DMA protocol to provide special functions. These lines change from the conventional to special definitions at the moment the Host decides to allow a DMA burst, if the Ultra DMA transfer mode was previously chosen via SetFeatures. The Drive becomes aware of this change upon assertion of the -DMACK line. These lines revert back to their original definitions upon the deassertion of -DMACK at the termination of the DMA burst.

	Special Definition (for Ultra DMA)	Conventional Definition
Write Operation	–DDMARDY HSTROBE STOP	IORDY –DIOR –DIOW
Read Operation	–HDMARDY DSTROBE STOP	–DIOR IORDY –DIOW

Figure 16. Signal Special Definitions for Ultra DMA

DD00-DD15 16-bit bi-directional data bus between the host and the HDD. The lower 8 lines, DD00-07, are used for Register and ECC access. All 16 lines, DD00-15, are used for data transfer. These are 3-State lines with 24 mA current sink capability.

DA00-DA02 Address used to select the individual register in the HDD.

-CS0 Chip select signal generated from the Host address bus. When active, one of the Command Block Registers (Data, Error{Features when written}, Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status{Command when written} register) can be selected.
(SeeFigure 39 on page 44 .)

-CS1 Chip select signal generated from the Host address bus. When active, one of the Control Block Registers (Alternate Status{Device Control when written} and Drive Address register) can be selected.
(SeeFigure 39 on page 44 .)

-RESET This line is used to reset the HDD. It shall be kept Low logic state during power up and kept High thereafter.

-DIOW Its rising edge holds data from the host data bus to a register or data register of the HDD.

-DIOR When low, this signal enables data from a register or data register of the drive onto data bus. The data on the bus shall be latched on the rising edge of -DIOR.

INTRQ Interrupt is enabled only when the drive is selected, and the host activates the -IEN bit in the Device Control Reg. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a host read of the status register or a write to the Command Reg. This signal is a 3-State line with 24 mA sink capability.

-HIOCS16 Indication to the host that a 16-bit wide data register has been addressed and that the drive is prepared to send or receive a 16-bit wide data word. This signal is an Open-Drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.

-DASP This is a time-multiplexed signal which indicates that a drive is active, or that device 1 is present. This signal is driven by Open-Drain driver and internally pulled-up to 5 volts through a 10kΩ resistor.
During Power-On initialization or after -RESET is negated, -DASP shall be asserted by Device 1 within 400 msec to indicate that device 1 is present. Device 0 shall allow up to 450msec for device 1 to assert -DASP. If device 1 is not present, device 0 may assert -DASP to drive a LED indicator.
-DASP shall be negated following acceptance of the first valid command by device 1.
Anytime after negation of -DASP, either drive may assert -DASP to indicate that a drive is active.

-PDIAG/-CBLID
-PDIAG shall be asserted by device 1 to indicate to device 0 that it has completed diagnostics. This line is pulled-up to 5 volts in the HDD through a 10kΩ resistor.
Following a Power On Reset, software reset or -RESET, drive 1 shall negate -PDIAG within 1 msec (to indicate to device 0 that it is busy). Drive 1 shall then assert -PDIAG within 30 seconds to indicate that it is no longer busy, and is able to provide status.
Following the receipt of a valid Execute Drive Diagnostics command, device 1 shall negate -PDIAG within 1 msec to indicate to device 0 that it is busy and has not yet passed its drive diagnostics. If device 1 is present then device 0 shall wait up to 6 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert -PDIAG. Device 1 should clear BSY before asserting -PDIAG, as -PDIAG is used to indicate that device 1 has passed its diagnostics and is ready to post status.
If -DASP was not asserted by device 1 during reset initialization, device 0 shall post its own status immediately after it completes diagnostics, and clear the device 1 Status register to

00h. Device 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).
Device 1 shall release -PDIAG/-CBLID no later than after the first command following a power on or hardware reset sequence so that the host may sample -PDIAG/-CBLIB in order to detect the presence or absence of an 80-conductor cable assembly.

CSEL (Cable Select) (Optional)

The drive is configured as either Device 0 or 1 depending upon the value of CSEL.

- If CSEL is grounded then the device address is 0.
- If CSEL is open then the device address is 1.

KEY Pin position 20 has no connection pin. It is recommended to close the respective position of the cable connector in order to avoid incorrect insertion by mistake.

IORDY This signal is negated to extend the host transfer cycle when a drive is not ready to respond to a data transfer request, and may be negated when the host transfer cycle is less than 240 nsec for PIO data transfer. This signal is an open-drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.

-DMACK This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

This signal is internally pulled-up to 5Volt through 15 K ohm resistor and the tolerance of the resistor value is -50% to +100%.

DMARQ This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by -HIOR and -HIOW. This signal is used on a handshake manner with -DMACK. This signal is a 3-state line with 24mA sink capability and internally pulled-down to GND through 10 kΩ resistor.

-HDMARDY (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

-HDMARDY is a flow control signal for Ultra DMA data in bursts. This signal is held asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data in transfers. The host may negate -HDMARDY to pause an Ultra DMA data in transfer.

HSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

HSTROBE is the data out strobe signal from the host for an Ultra DMA data out transfer. Both the rising and falling edge of HSTROBE latch the data from DD(15:0) into the device. The host may stop toggling HSTROBE to pause an Ultra DMA data out transfer.

STOP (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

STOP shall be asserted by the host prior to initiation of an Ultra DMA burst. STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during or after data transfer in an Ultra DMA mode signals the termination of the burst.

-DDMARDY (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

-DDMARDY is a flow control signal for Ultra DMA data out bursts. This signal is held asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data out transfers. The device may negate -DDMARDY to pause an Uptra DMA data out transfer.

DSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

DSTROBE is the data int strobe signal from the device for an Ultra DMA data in transfer. Both the rising and falling edge of DSTROBE latch the data from DD(15:0) into the host. The device may stop toggling DSTROBE to pause an Ultra DMA data in transfer.

Note : The termination resistors at the device side are implemented as follows :

Device Termination (implemented on HDD side)

- 33 ohm for DD0 thru DD15, DMARQ, INTRQ
- 82 ohm for -CS0, -CS1, DA00, DA01, DA02, -DIOR, DIOW, -DMACK
- 22 ohm for IORDY

6.1.3 Interface Logic Signal Levels

The interface logic signal has the following electrical specifications:

Inputs :	Input High Voltage	–	2.0 V min.
	Input Low Voltage	–	0.8 V max.
Outputs :	Output High Voltage	–	2.4 V min.
	Output Low Voltage	–	0.5 V max.

6.2 Signal Timings

6.2.1 Reset Timings

HDD reset timing.

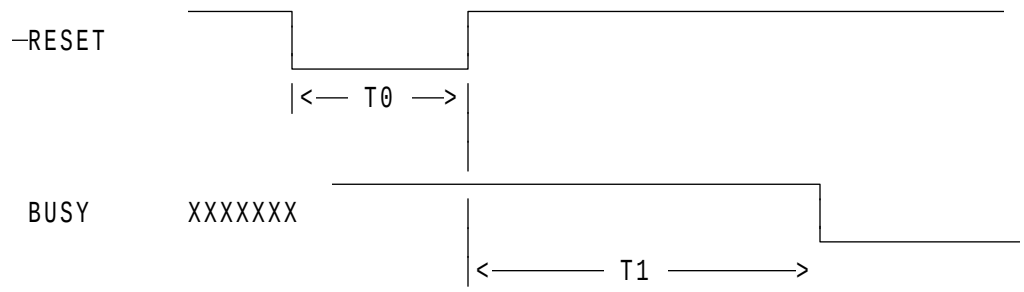


Figure 17. System Reset timing chart

	PARAMETER DESCRIPTION	Min (usec)	Max (sec)
T0	–RESET low width	25	
T1	–RESET high to not BUSY	—	31

Figure 18. System Reset timing

6.2.2 PIO Timings

The PIO cycle timings meet Mode 4 of the ATA/ATAPI-4 description.

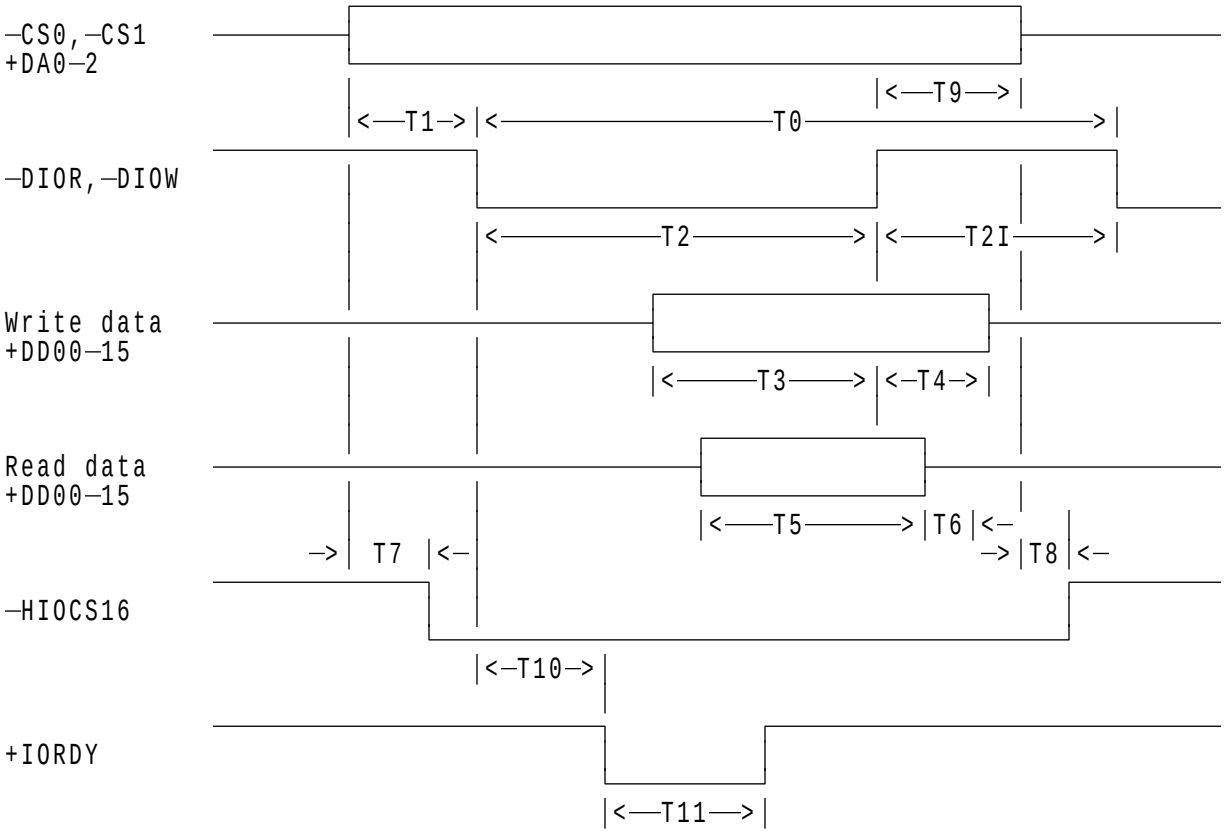


Figure 19. PIO cycle time chart

	PARAMETER DESCRIPTION	MIN (nsec)	MAX (nsec)	Note
T0	Cycle time	120	–	
T1	–CS0–1, +DA00–02 valid to –DIOR,–DIOW active	25	–	
T2	–DIOR,–DIOW pulse width	70	–	
T2I	–DIOR,–DIOW recovery	25	–	
T3	+DD00–15 setup to –DIOW high	20	–	
T4	–DIOW high to +DD00–15 hold	10	–	
T5	+DD00–15 setup to –DIOR high	20	–	
T6	–DIOR high to +DD00–15 hold	5	–	
T7	–CS0–1, +DA00–02 valid to –HIOCS16 assertion	–	40	
T8	–CS0–1, +DA00–02 invalid to –HIOCS16 negation	–	30	
T9	–DIOR,–DIOW high to –CS0–1, +DA00–02 hold	10		
T10	–DIOR,–DIOW low to +IORDY low	–	35	
T11	+IORDY pulse width	–	1250	

Figure 20. PIO cycle timings

6.2.2.1 Write DRQ Interval Time

For write sectors and write multiple operations, 4.8µsec is inserted from the end of negation of the DRQ bit until setting of the next DRQ bit.

6.2.2.2 Read DRQ Interval Time

For read sectors and read multiple operations, the interval from the end of negation of the DRQ bit until setting of the next DRQ bit is as follows;

- In case that a host reads the status register only before the sector or block transfer DRQ interval

  DRQ interval ..... 5.2µsec.

- In case that a host reads the status register after or both before and after the sector or block transfer

  DRQ interval ..... 14.4µsec.

6.2.3 DMA Timings

6.2.3.1 Multiword DMA Timings

The Multiword DMA timing meets Mode 2 of the ATA-4 description.

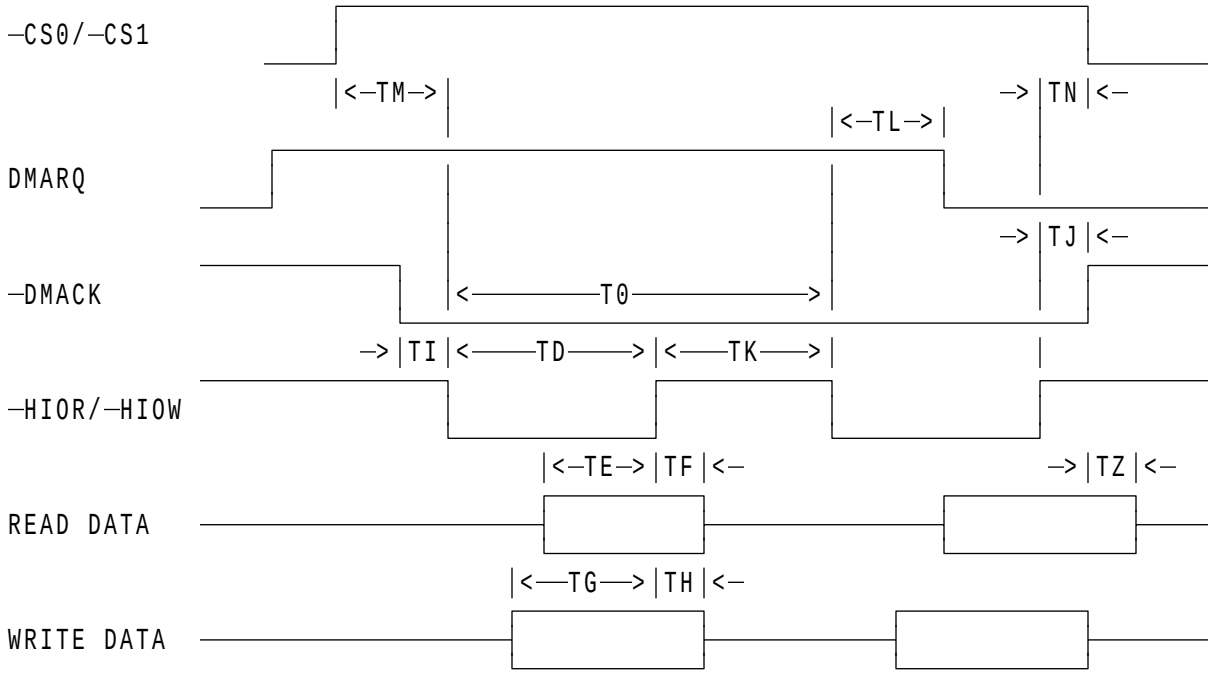


Figure 21. Multiword DMA cycle time chart

[nsec]

	PARAMETER DESCRIPTION	MIN	MAX	Note
T0	Cycle time	120	–	
TD	–HIOR,–HIOW pulse width	70	–	
TE	–HIOR data setup	50	–	
TF	–HIOR data hold	5	–	
TG	–HIOW data setup	20	–	
TH	–HIOW data hold	10	–	
TI	–DMACK to –HIOR/–HIOW setup	0	–	
TJ	–HIOR/–HIOW to –DMACK hold	5	–	
TK	–HIOR/–HIOW nagated pulse width	25	–	
TL	–HIOR/–HIOW to –DMARQ delay	–	35	
TM	–CS0/–CS1 valid to –DIOR/–DIOW	25	–	
TN	–CS0/–CS1 hold	10	–	
TZ	–DMACK to tristate	–	25	

Figure 22. Multiword DMA cycle timings

6.2.4 Ultra DMA Timings

The Ultra DMA timing meets Mode 0,1,2,3 and 4 of the Ultra DMA Protocol.

6.2.4.1 Initiating Read DMA

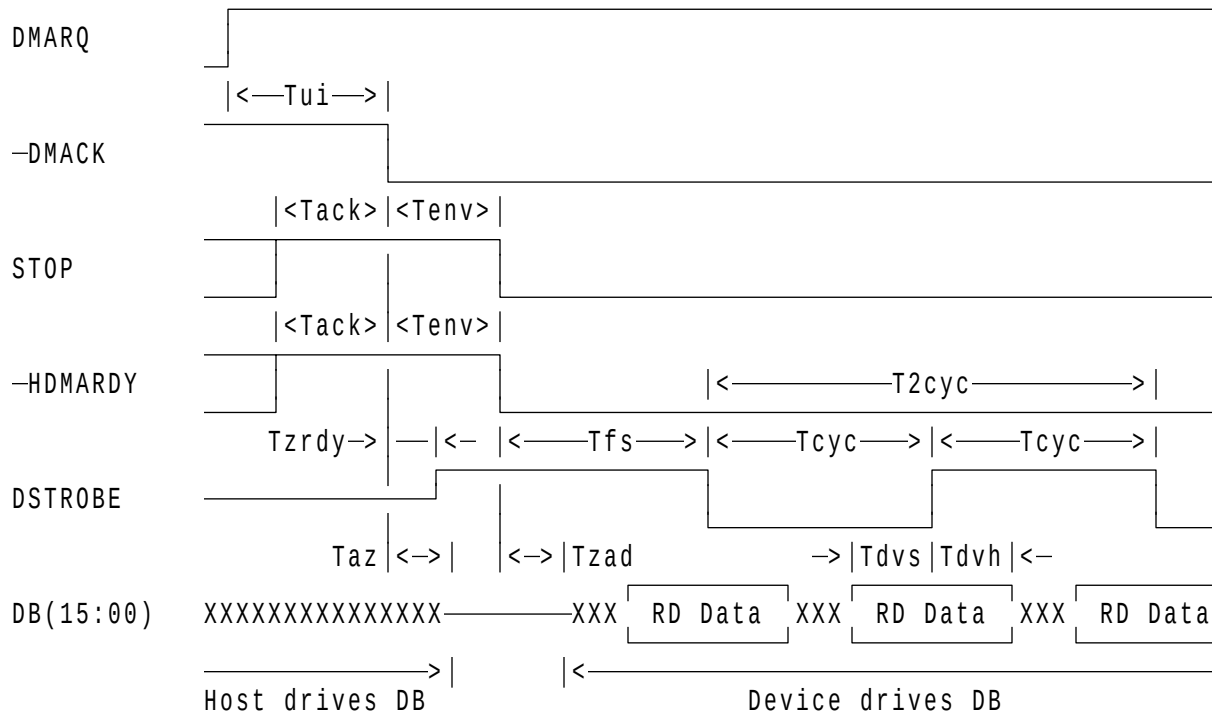


Figure 23. Ultra DMA cycle time chart (Initiating Read)

[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tui	Unlimited interlock time	0	—	0	—	0	—
Tack	Setup time before —DMACK assertion	20	—	20	—	20	—
Tenv	Envelope time	20	70	20	70	20	70
Tzrdy	Wait time before driving DSTROBE	0	—	0	—	0	—
Tfs	First strobe time	0	230	0	200	0	170
Tcyc	Cycle Time	112	—	73	—	54	—
T2cyc	2 Cycle time	230	—	154	—	115	—
Taz	Output release time	—	10	—	10	—	10
Tzad	Output enable time	0	—	0	—	0	—
Tdvs	Data setup time (at device side)	70	—	48	—	30	—
Tdvh	Data Hold time (at device side)	6	—	6	—	6	—

[nsec]

	PARAMETER DESCRIPTION	MODE3		MODE4	
		MIN	MAX	MIN	MAX
Tui	Unlimited interlock time	0	—	0	—
Tack	Setup time before —DMACK assertion	20	—	20	—
Tenv	Envelope time	20	55	20	55
Tzrdy	Wait time before driving DSTROBE	0	—	0	—
Tfs	First strobe time	0	130	0	120
Tcyc	Cycle Time	39	—	25	—
T2cyc	2 Cycle time	86	—	57	—
Taz	Output release time	—	10	—	10
Tzad	Output enable time	0	—	0	—
Tdvs	Data setup time (at device side)	20	—	6	—
Tdvh	Data Hold time (at device side)	6	—	6	—

Figure 24. Ultra DMA cycle timings (Initiating Read)

6.2.4.2 Host Pausing Read DMA

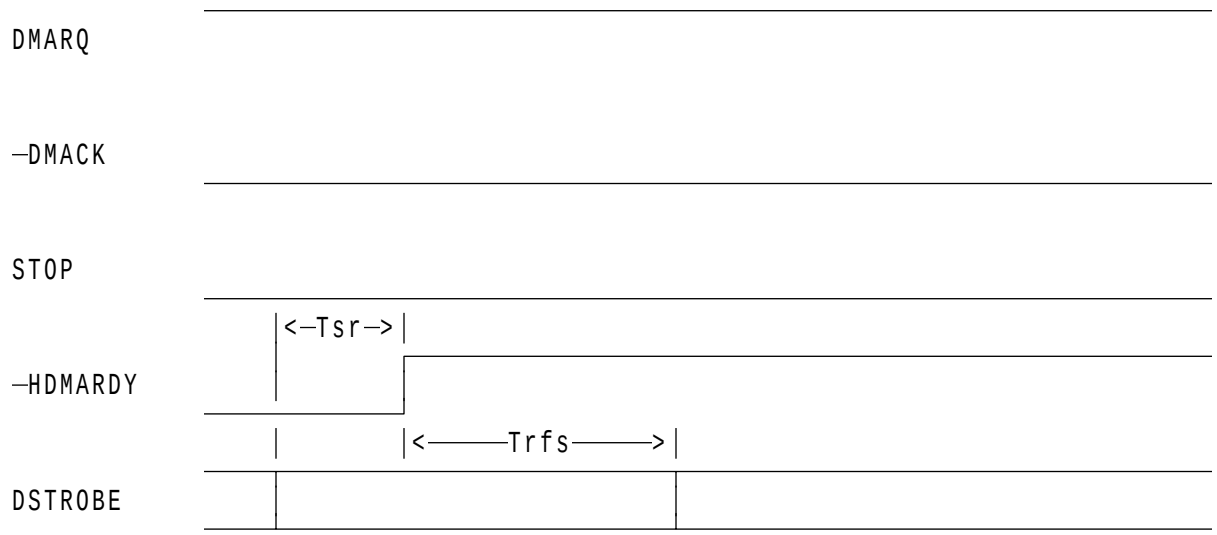


Figure 25. Ultra DMA cycle time chart (Host pausing Read)

[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tsr	Strobe to ready response time	–	50	–	30	–	20
Trfs	Ready to final strobe time	–	75	–	70	–	60

[nsec]

	PARAMETER DESCRIPTION	MODE3		MODE4	
		MIN	MAX	MIN	MAX
Tsr	Strobe to ready response time	–	–	–	–
Trfs	Ready to final strobe time	–	60	–	60

Note : When a host does not meet Tsr, it should be ready to receive 2 (mode 0, 1 and 2) or 3 (mode 3 and 4) more strobes after –HDMARDY is negated.

Figure 26. Ultra DMA cycle timings (Host pausing Read)

6.2.4.3 Host Terminating Read DMA

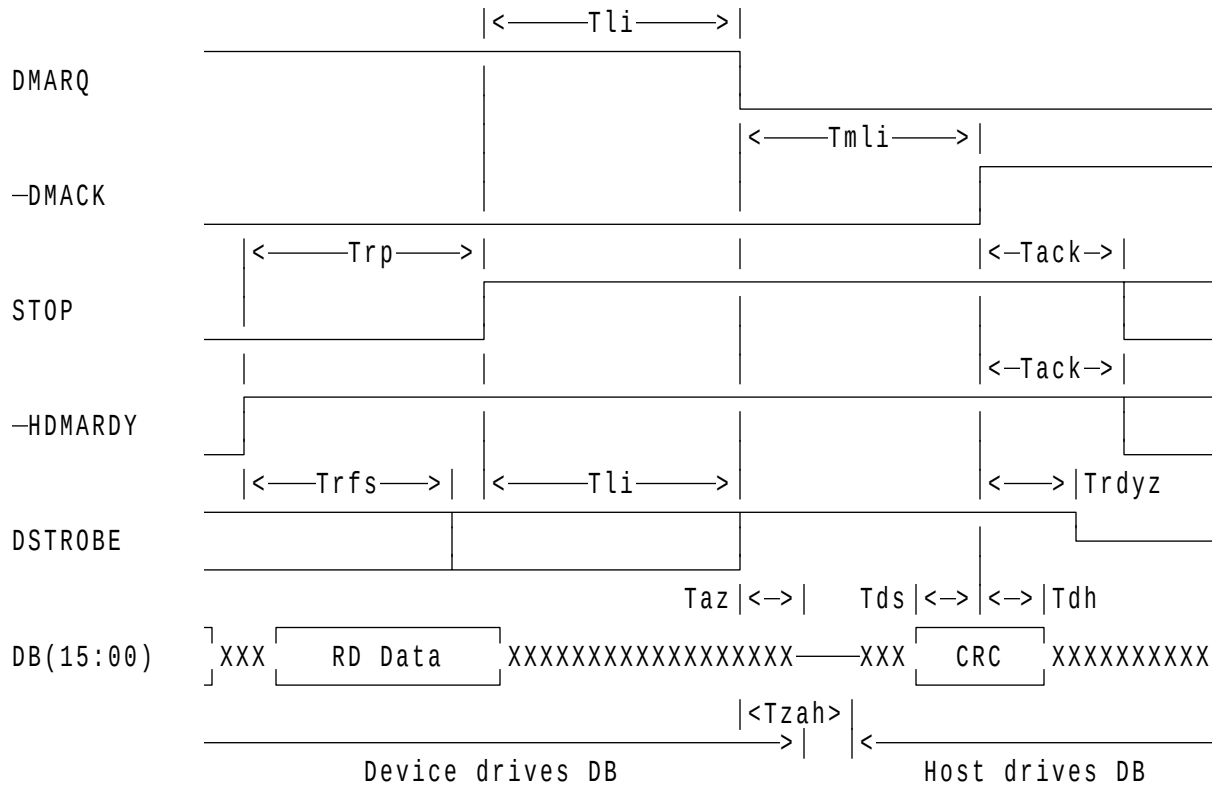


Figure 27. Ultra DMA cycle time chart (Host terminating Read)

[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Trfs	Ready to final strobe time	—	75	—	70	—	60
Trp	Ready to pause time	160	—	125	—	100	—
Tli	Limited interlock time	0	150	0	150	0	150
Taz	Output release time	—	10	—	10	—	10
Tzah	Output enable time	20	—	20	—	20	—
Tmli	Interlock time	20	—	20	—	20	—
Tds	Data setup time (at device side)	15	—	10	—	7	—
Tdh	Data Hold time (at device side)	5	—	5	—	5	—
Tack	Hold time after —DMACK negation	20	—	20	—	20	—
Trdyz	Pull—up time before DSTROBE release	—	20	—	20	—	20

[nsec]

	PARAMETER DESCRIPTION	MODE3		MODE4	
		MIN	MAX	MIN	MAX
Trfs	Ready to final strobe time	—	60	—	60
Trp	Ready to pause time	100	—	100	—
Tli	Limited interlock time	0	100	0	100
Taz	Output release time	—	10	—	10
Tzah	Output enable time	20	—	20	—
Tmli	Interlock time	20	—	20	—
Tds	Data setup time (at device side)	7	—	5	—
Tdh	Data Hold time (at device side)	5	—	5	—
Tack	Hold time after —DMACK negation	20	—	20	—
Trdyz	Pull—up time before DSTROBE release	—	20	—	20

Figure 28. Ultra DMA cycle timings (Host terminating Read)

6.2.4.4 Device Terminating Read DMA

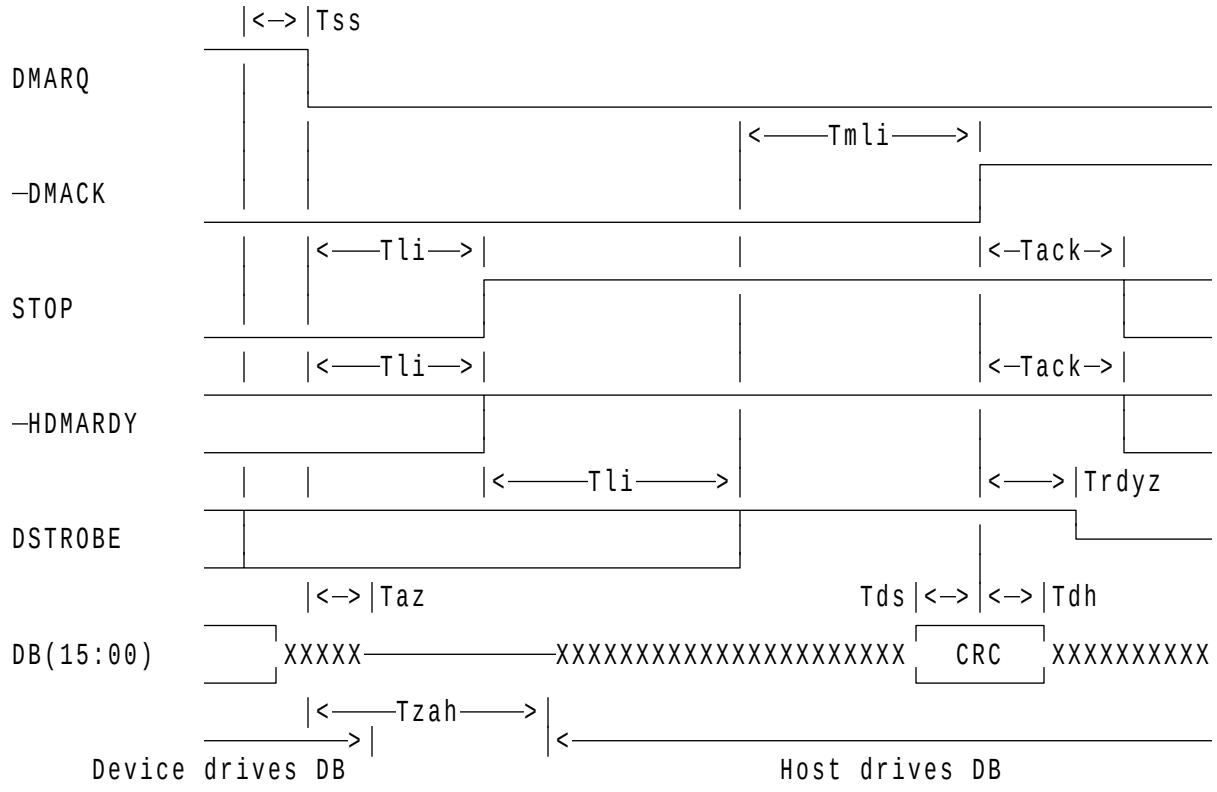


Figure 29. Ultra DMA cycle time chart (Device terminating Read)

[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tss	Time from strobe to stop assertion	50	–	50	–	50	–
Tli	Limited interlock time	0	150	0	150	0	150
Taz	Output release time	–	10	–	10	–	10
Tzah	Output enable time	20	–	20	–	20	–
Tmli	Interlock time	20	–	20	–	20	–
Tds	Data setup time (at device side)	15	–	10	–	7	–
Tdh	Data Hold time (at device side)	5	–	5	–	5	–
Tack	Hold time after –DMACK negation	20	–	20	–	20	–
Trdyz	Pull–up time before DSTROBE release	–	20	–	20	–	20

[nsec]

	PARAMETER DESCRIPTION	MODE3		MODE4	
		MIN	MAX	MIN	MAX
Tss	Time from strobe to stop assertion	50	–	50	–
Tli	Limited interlock time	0	100	0	100
Taz	Output release time	–	10	–	10
Tzah	Output enable time	20	–	20	–
Tmli	Interlock time	20	–	20	–
Tds	Data setup time (at device side)	7	–	5	–
Tdh	Data Hold time (at device side)	5	–	5	–
Tack	Hold time after –DMACK negation	20	–	20	–
Trdyz	Pull–up time before DSTROBE release	–	20	–	20

Figure 30. Ultra DMA cycle timings (Device terminating Read)

6.2.4.5 Initiating Write DMA

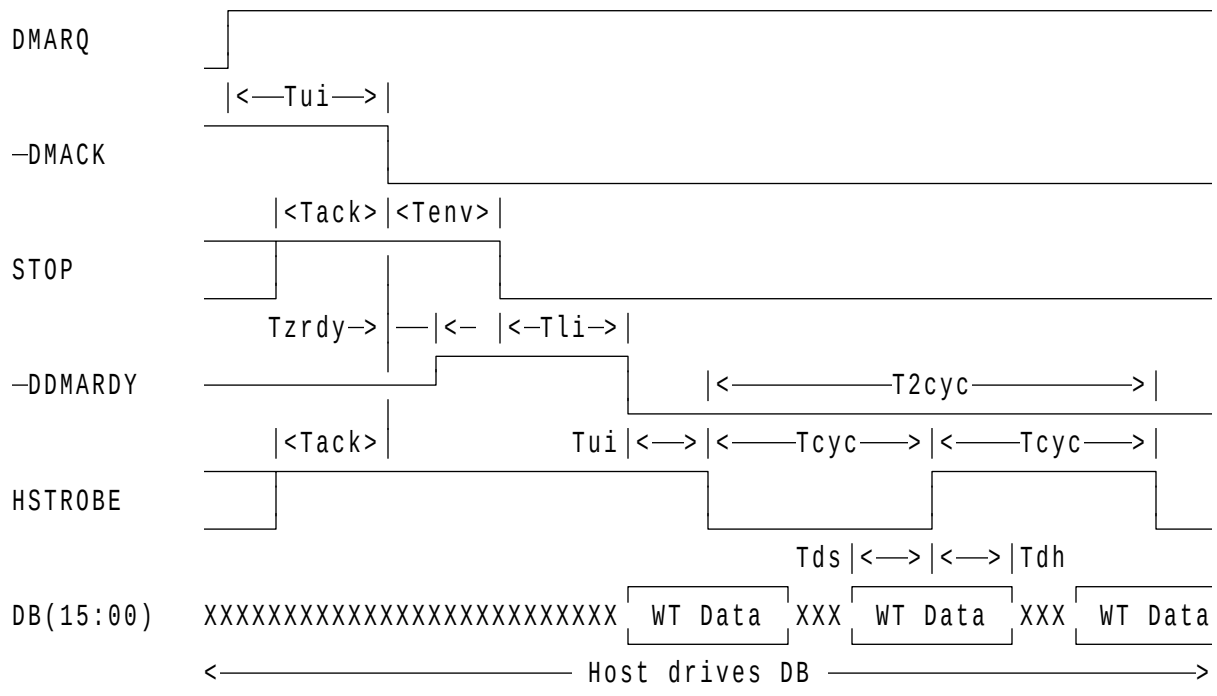


Figure 31. Ultra DMA cycle time chart (Initiating Write)

[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tui	Unlimited interlock time	0	—	0	—	0	—
Tack	Setup time before —DMACK assertion	20	—	20	—	20	—
Tenv	Envelope time	20	70	20	70	20	70
Tzrdy	Wait time before driving DSTROBE	0	—	0	—	0	—
Tli	Limited interlock time	0	150	0	150	0	150
Tcyc	Cycle Time	112	—	73	—	54	—
T2cyc	2 Cycle time	230	—	154	—	115	—
Tds	Data setup time (at device side)	15	—	10	—	7	—
Tdh	Data Hold time (at device side)	5	—	5	—	5	—

[nsec]

	PARAMETER DESCRIPTION	MODE3		MODE4	
		MIN	MAX	MIN	MAX
Tui	Unlimited interlock time	0	—	0	—
Tack	Setup time before —DMACK assertion	20	—	20	—
Tenv	Envelope time	20	55	20	55
Tzrdy	Wait time before driving DSTROBE	0	—	0	—
Tli	Limited interlock time	0	100	0	100
Tcyc	Cycle Time	39	—	25	—
T2cyc	2 Cycle time	86	—	57	—
Tds	Data setup time (at device side)	7	—	5	—
Tdh	Data Hold time (at device side)	5	—	5	—

Figure 32. Ultra DMA cycle timings (Initiating Write)

6.2.4.6 Device Pausing Write DMA

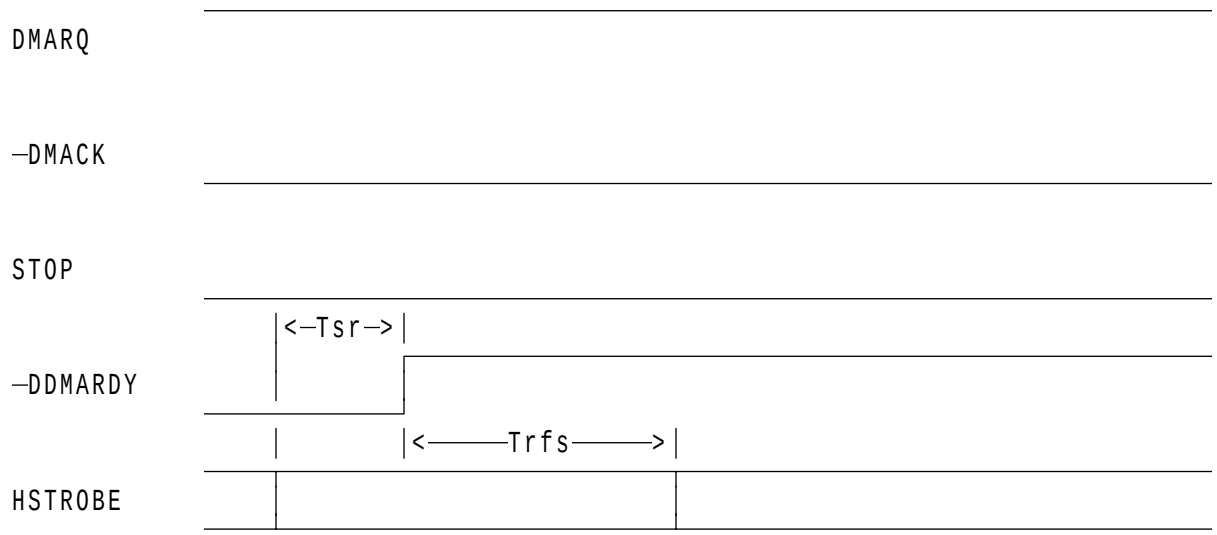


Figure 33. Ultra DMA cycle time chart (Device pausing Write)

[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tsr	Strobe to ready response time	—	50	—	30	—	20
Trfs	Ready to final strobe time	—	75	—	70	—	60

[nsec]

	PARAMETER DESCRIPTION	MODE3		MODE4	
		MIN	MAX	MIN	MAX
Tsr	Strobe to ready response time	—	—	—	—
Trfs	Ready to final strobe time	—	60	—	60

Note : When a device does not meet Tsr, it shall be ready to receive 3 more strobes after —DDMARDY is negated.

Figure 34. Ultra DMA cycle timings (Device pausing Write)

6.2.4.7 Device Terminating Write DMA

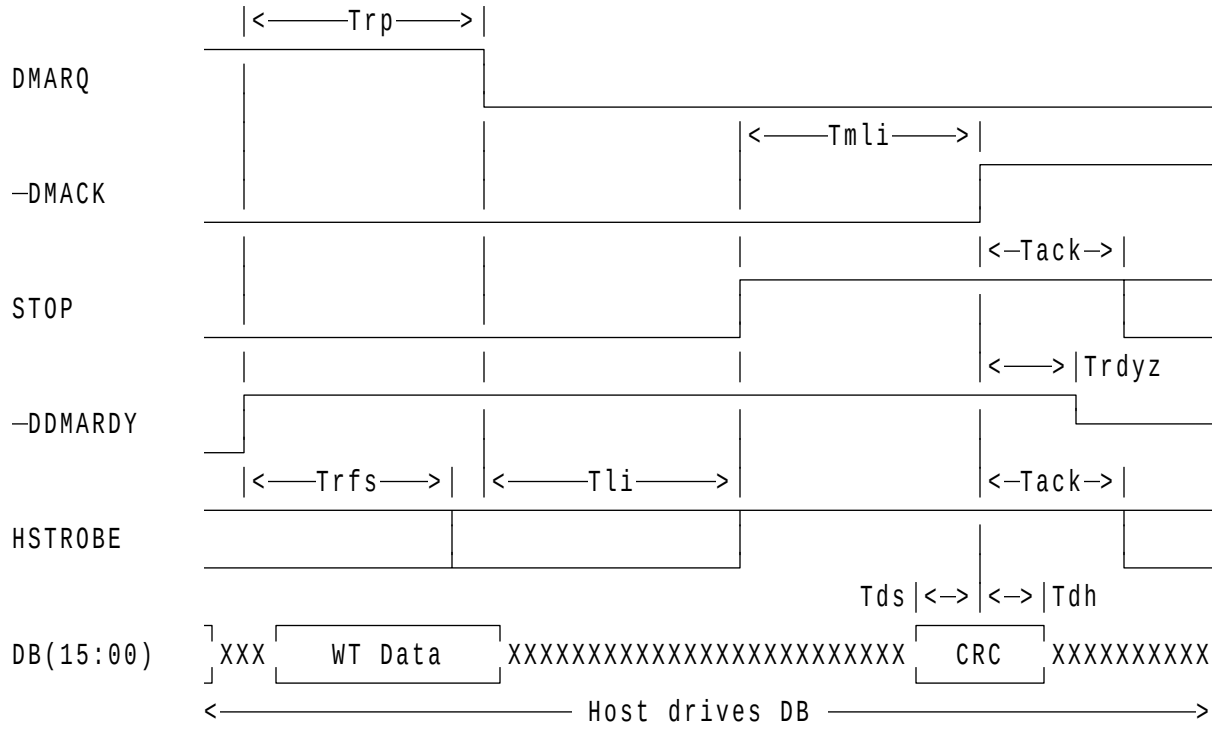


Figure 35. Ultra DMA cycle time chart (Device terminating Write)

[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Trfs	Ready to final strobe time	—	75	—	70	—	60
Trp	Ready to pause time	160	—	125	—	100	—
Tli	Limited interlock time	0	150	0	150	0	150
Tmli	Interlock time	20	—	20	—	20	—
Tds	Data setup time (at device side)	15	—	10	—	7	—
Tdh	Data Hold time (at device side)	5	—	5	—	5	—
Tack	Hold time after —DMACK negation	20	—	20	—	20	—
Trdyz	Pull—up time before HSTROBE release	—	20	—	20	—	20

[nsec]

	PARAMETER DESCRIPTION	MODE3		MODE4	
		MIN	MAX	MIN	MAX
Trfs	Ready to final strobe time	—	60	—	60
Trp	Ready to pause time	100	—	100	—
Tli	Limited interlock time	0	100	0	100
Tmli	Interlock time	20	—	20	—
Tds	Data setup time (at device side)	7	—	5	—
Tdh	Data Hold time (at device side)	5	—	5	—
Tack	Hold time after —DMACK negation	20	—	20	—
Trdyz	Pull—up time before HSTROBE release	—	20	—	20

Figure 36. Ultra DMA cycle timings (Device terminating Write)

6.2.4.8 Host Terminating Write DMA

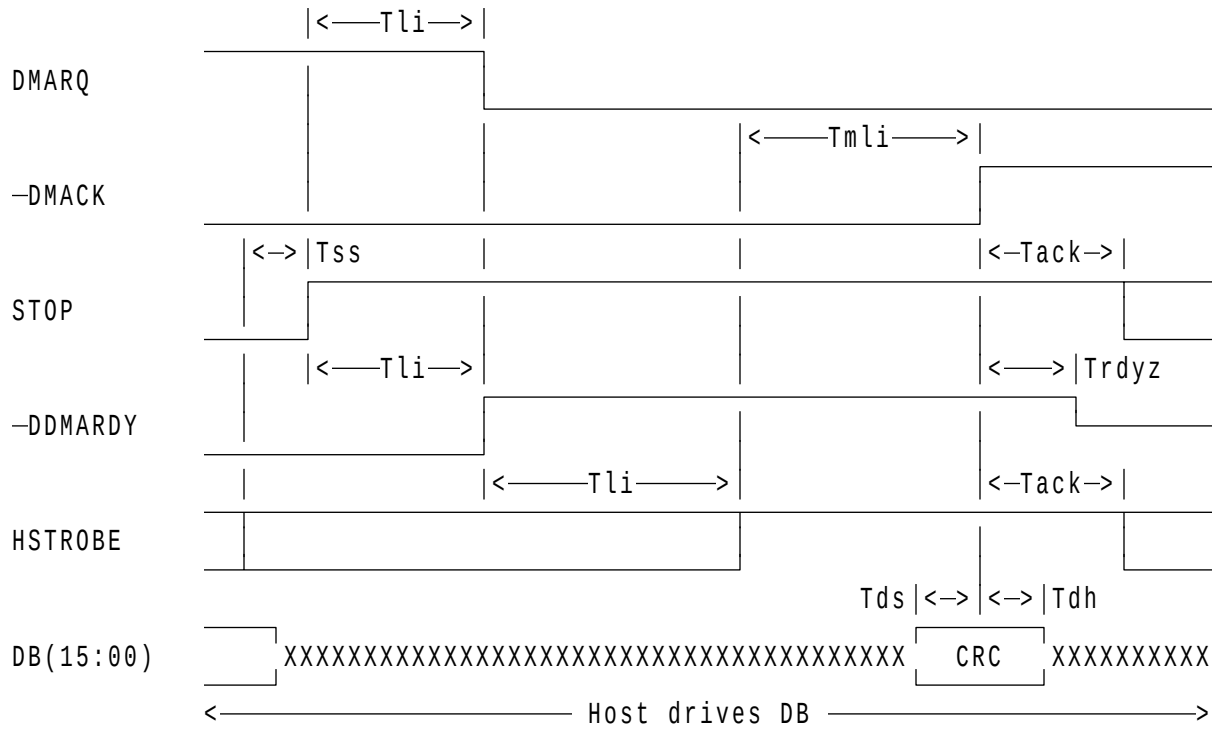


Figure 37. Ultra DMA cycle time chart (Host terminating Write)

[nsec]

	PARAMETER DESCRIPTION	MODE0		MODE1		MODE2	
		MIN	MAX	MIN	MAX	MIN	MAX
Tss	Time from strobe to stop assertion	50	—	50	—	50	—
Tli	Limited interlock time	0	150	0	150	0	150
Tmli	Interlock time	20	—	20	—	20	—
Tds	Data setup time (at device side)	15	—	10	—	7	—
Tdh	Data Hold time (at device side)	5	—	5	—	5	—
Tack	Hold time after —DMACK negation	20	—	20	—	20	—
Trdyz	Pull—up time before DSTROBE release	—	20	—	20	—	20

[nsec]

	PARAMETER DESCRIPTION	MODE3		MODE4	
		MIN	MAX	MIN	MAX
Tss	Time from strobe to stop assertion	50	—	50	—
Tli	Limited interlock time	0	100	0	100
Tmli	Interlock time	20	—	20	—
Tds	Data setup time (at device side)	7	—	5	—
Tdh	Data Hold time (at device side)	5	—	5	—
Tack	Hold time after —DMACK negation	20	—	20	—
Trdyz	Pull—up time before DSTROBE release	—	20	—	20

Figure 38. Ultra DMA cycle timings (Host terminating Write)

6.2.5 Addressing of HDD Registers

The host addresses the drive through a set of registers called the Task File. These registers are mapped into the host's I/O space. Two chip select lines (-CS0 and -CS1) and three address lines (DA00-02) are used to select one of these registers, while a -DIOR or -DIOW is provided at the specified time.

The -CS0 is used to address Command Block registers. while the -CS1 is used to address Control Block registers.

The following table shows the I/O address map.

–CS0	–CS1	DA02	DA01	DA00	–DIOR = 0 (Read)	–DIOW = 0 (Write)
					Command Block Registers	
0	1	0	0	0	Data Reg.	Data Reg.
0	1	0	0	1	Error Reg.	Features Reg.
0	1	0	1	0	Sector count Reg.	Sector count Reg.
0	1	0	1	1	Sector number Reg.	Sector number Reg
0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
0	1	1	1	0	Drive/Head Reg.	Drive/Head Reg.
0	1	1	1	1	Status Reg.	Command Reg.
					Control Block Registers	
1	0	1	1	0	Alt. Status Reg.	Device control Reg
1	0	1	1	1	Drive address Reg.	–

Figure 39. I/O address map

Note: "Addr." field is shown just as an example.

During DMA operation (from writing to the command register until an interrupt), all registers are not accessible.

For example, the host is not supposed to read status register contents before interrupt (the value is invalid).

6.2.6 Cabling

The maximum cable length from the host system to the HDD plus circuit pattern length in the host system shall not exceed 18 inches.

For higher data transfer application(>8.3MB/sec), a consideration in system design is recommended to reduce cable noise and/or cross-talk, such as shorter cable, bus termination, shielded cable, etc.

For systems operating with Ultra DMA mode 3 or 4, 80-conductor ATA cable assembly (SFF-8049) shall be used.

6.3 Jumper Settings

6.3.1 Location of Jumper Pin

Jumper pins are located between power pins and AT interface pins.
Refer to 6.7.3, “ Connector Locations” on page 59 for location of the jumper pins. Pin position A is indicated in the figure.

6.3.2 Jumper Pin Assignment

Pin number A through I are prepared for jumper setting.

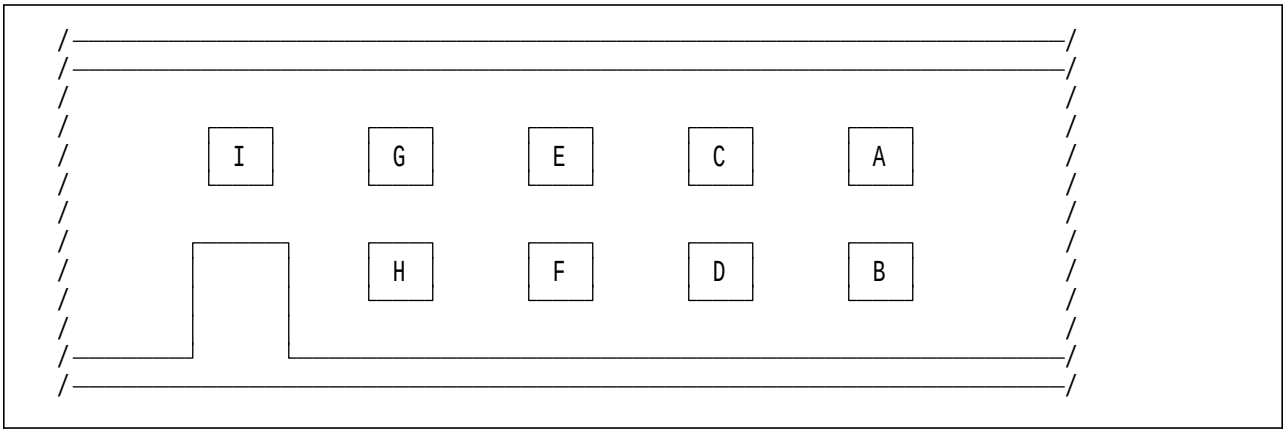


Figure 40. Jumper Pin Assignment

6.3.3 Jumper Function

Device 0, Device 1, Cable Select, and Device 0 Forcing Device 1 Present can be selected exclussively with one of the following conditions.

- Default Logical Head 16
- Default Logical Head 15
- Capacity Clip to 2GB (Default Logical Head 16)
- Disable Auto Spin (Default Logical Head 16)

6.3.4 Jumper Set Position

6.3.4.1 For Default Logical Head 16

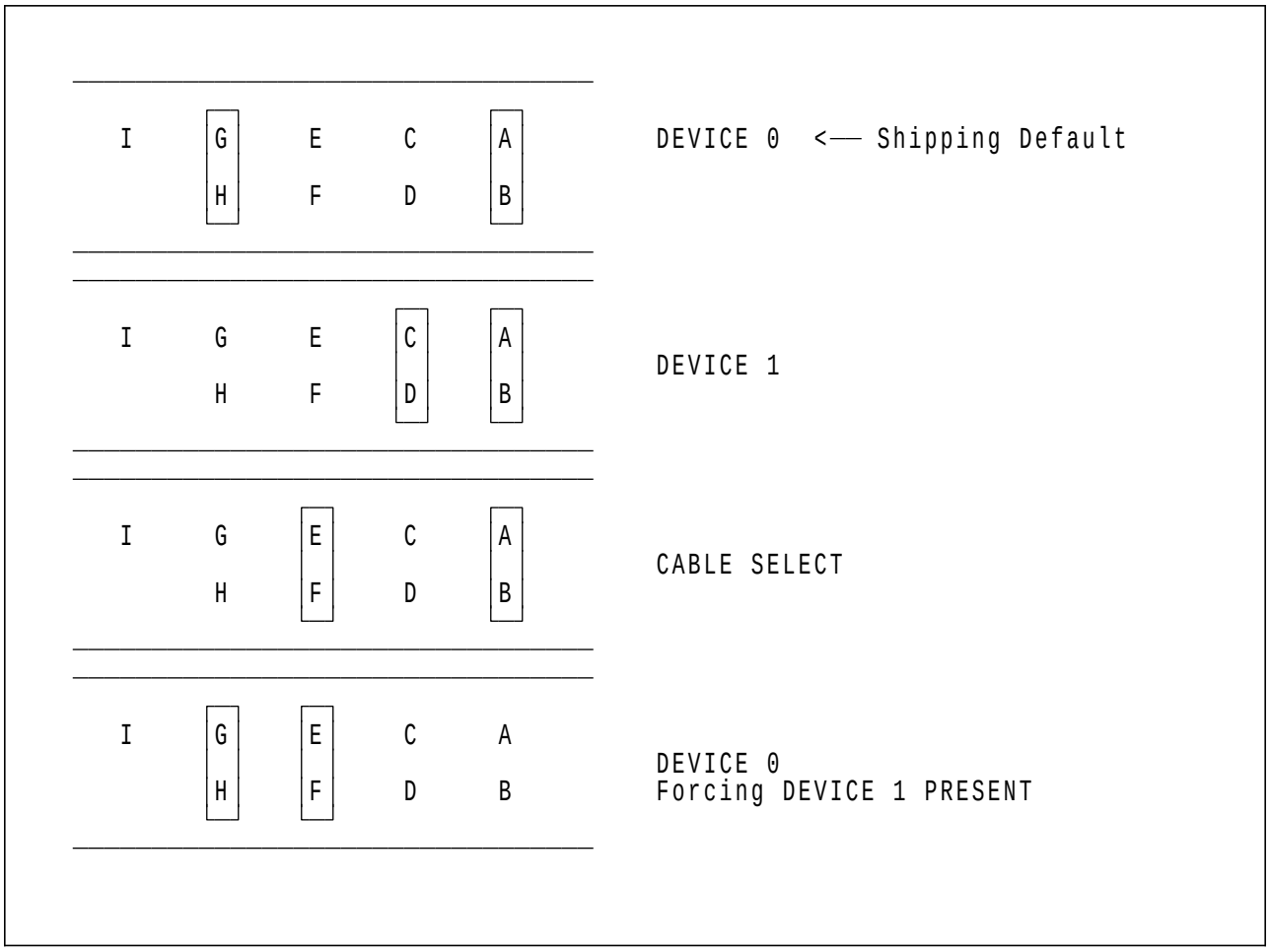


Figure 41. Jumper Block Setting Position

Notes:

1. All other setting patterns are reserved. Do not make other setting.
2. When CABLE SELECT is specified, AT interface signal #28 CSEL is referred to determin the drive address as follows:
   - When CSEL is grounded or at a low level, the drive address is 0 (Device0).
   - When CSEL is open or at a high level, the drive address is 1 (Device1).

6.3.4.2 For Default Logical Head 15

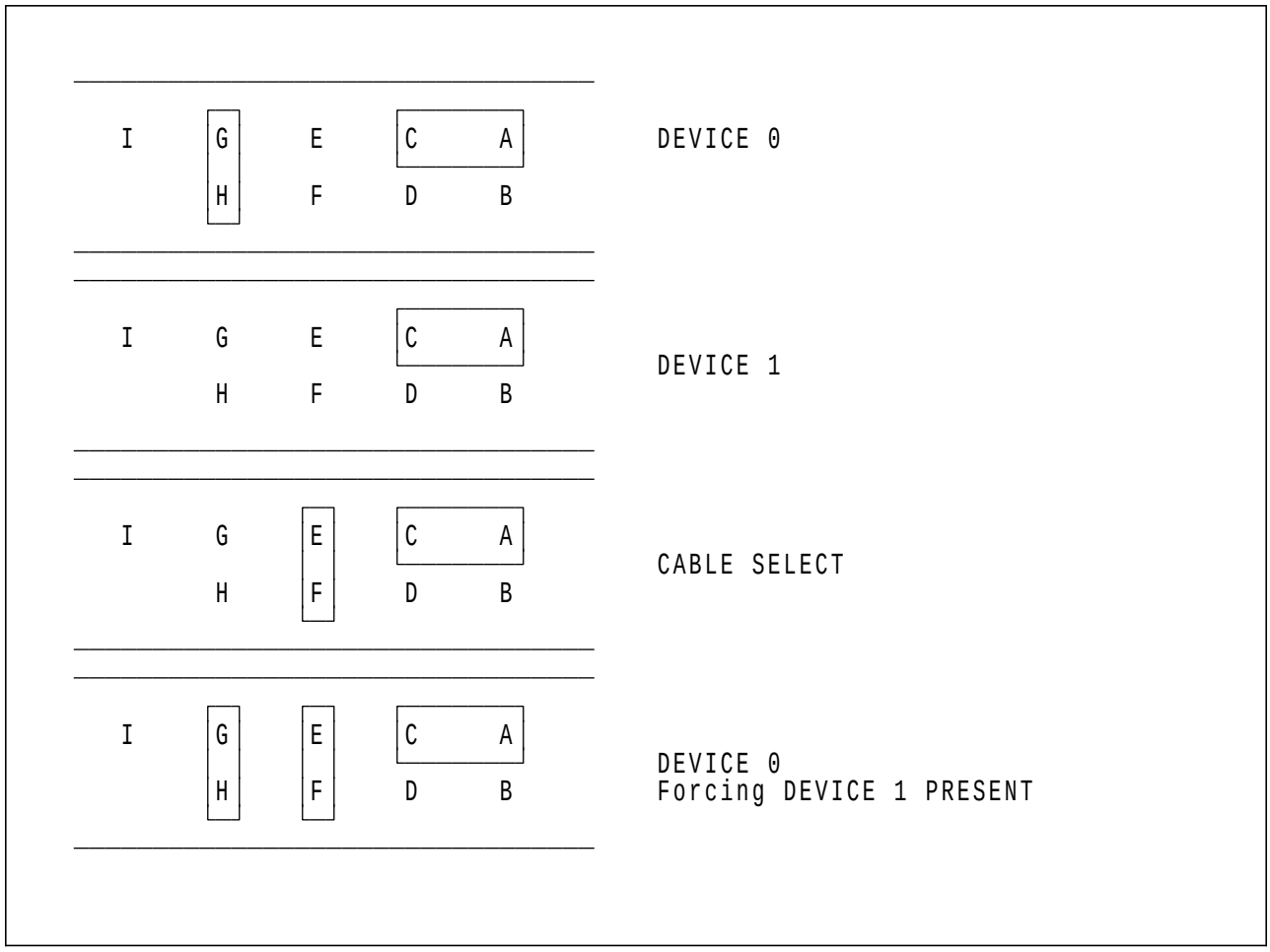


Figure 42. Jumper Block Setting Position

Notes:

1. All other setting patterns are reserved. Do not make other setting.
2. When CABLE SELECT is specified, AT interface signal #28 CSEL is referred to determin the drive address as follows:
   - When CSEL is grounded or at a low level, the drive address is 0 (Device0).
   - When CSEL is open or at a high level, the drive address is 1 (Device1).

6.3.4.3 For Capacity Clip to 2GB with Default Logical Head 16

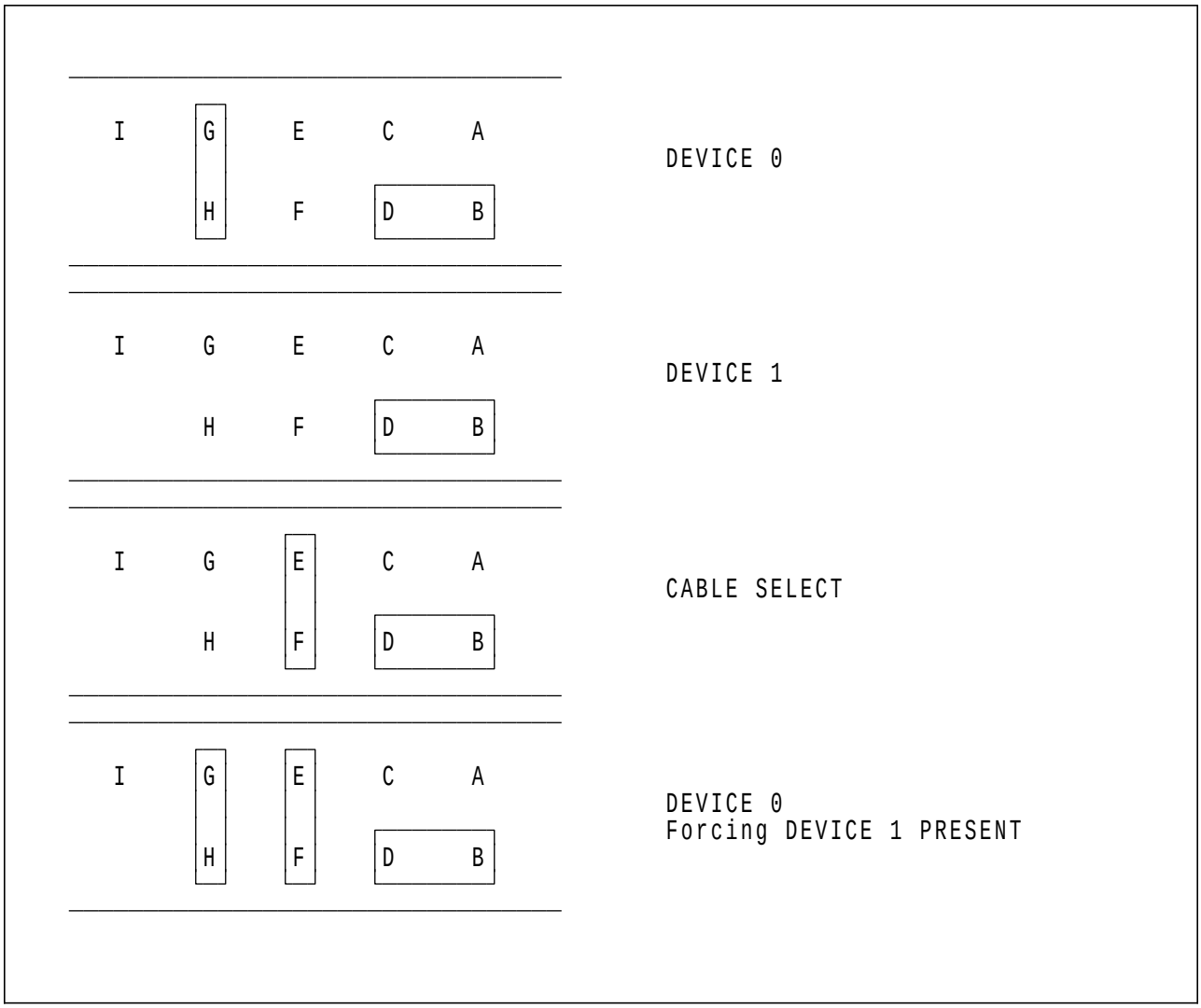


Figure 43. Jumper Block Setting Position

Notes:

1. All other setting patterns are reserved. Do not make other setting.
2. When CABLE SELECT is specified, AT interface signal #28 CSEL is referred to determin the drive address as follows:
   - When CSEL is grounded or at a low level, the drive address is 0 (Device0).
   - When CSEL is open or at a high level, the drive address is 1 (Device1).

6.3.4.4 For Disabling Auto Spin with Default Logical Head 16

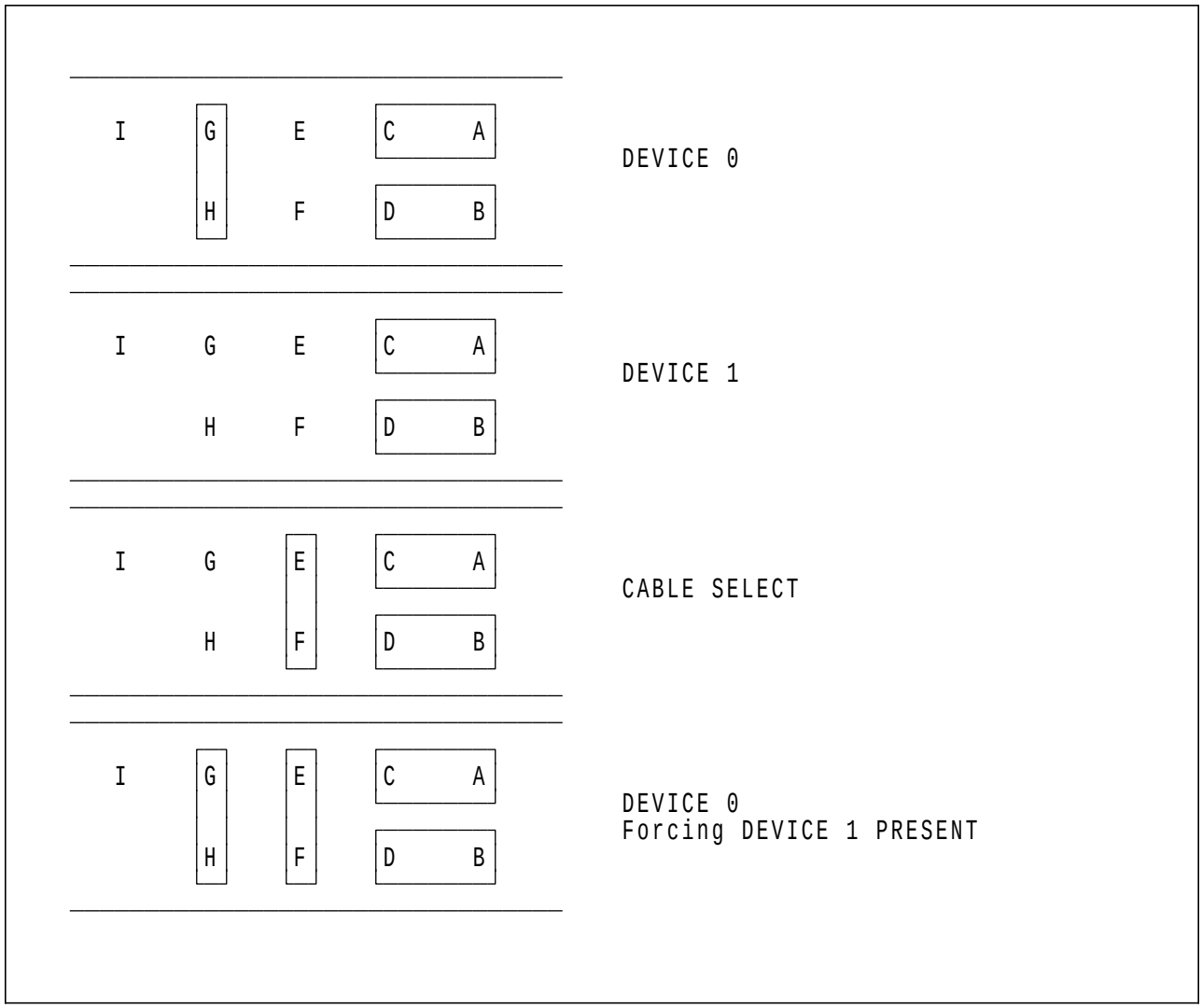


Figure 44. Jumper Block Setting Position

Notes:

1. All other setting patterns are reserved. Do not make other setting.
2. When CABLE SELECT is specified, AT interface signal #28 CSEL is referred to determin the drive address as follows:
   - When CSEL is grounded or at a low level, the drive address is 0 (Device0).
   - When CSEL is open or at a high level, the drive address is 1 (Device1).

6.4 Environment

Figure 45. Environmental Condition	
Operating Conditions	
Temperature	5 to 55 ˚C (See note)
Relative Humidity	8 to 90 %RH
Maximum Wet Bulb Temperature	29.4 ˚C
Maximum Temperature Gradient	15 ˚C / Hour
Altitude	– 300 to 3048 m
Non-Operating Conditions	
Temperature	– 40 to 65 ˚C
Relative Humidity	5 to 95 %RH
Maximum Wet Bulb Temperature	35 ˚C
Maximum Temperature Gradient	15 ˚C / Hour
Altitude	– 300 to 12,000 m

Note:

The system has to provide sufficient ventilation to maintain a surface temperature below 60[˚C] at the center of drive top cover.

Non-condensing should be kept at any time.

Maximum storage period with shipping package is one year.

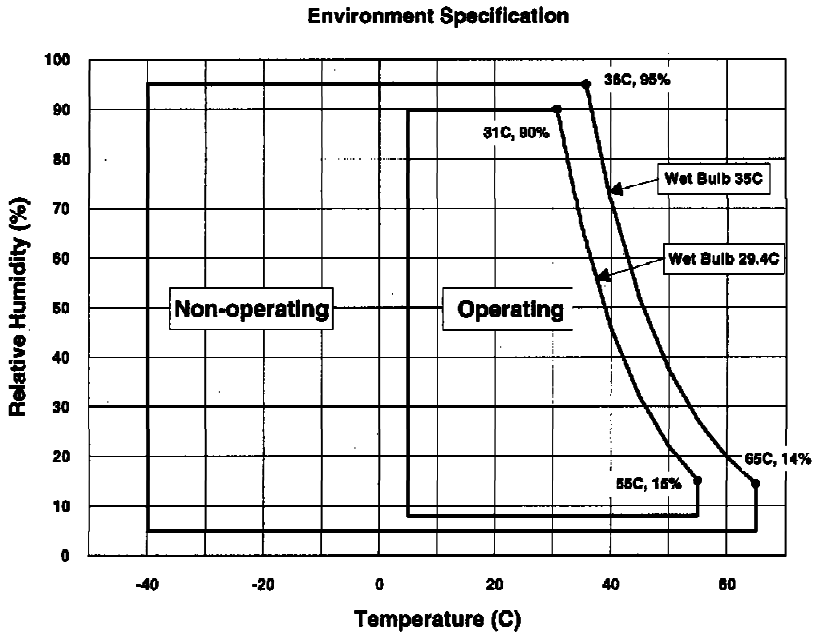


Figure 46. Limits of Temperature and Humidity

6.5 DC Power Requirements

Connection to the product should be made in isolated secondary circuits (SELV). The following voltage specification is applied at the power connector of the drive. Damage to the file electronics may result if the power supply cable is connected or disconnected while power is being applied to the file **(Hot plug/unplug is not allowed)**. There is no special power on/off sequencing required.

Figure 47. Input Voltage

	During run and spin up	Absolute max voltage
+5 Volts Supply	5V +/-5%	7V
+12 Volts Supply	12V +10%,-8%	15V

Figure 48. Power Supply Current of DJNA-372200/371800

(All values in Amps.)	+5Volts		+12Volts		Total (W)
	Pop Mean	Std.Dev	Pop Mean	Std.Dev	
Idle Average	0.25	0.02	0.42	0.04	6.9
Idle ripple (peak-to-peak)	0.31	0.02	0.89	0.08	
Seek peak	0.49	0.03	1.96	0.08	
Seek average (*1)	0.29	0.02	0.62	0.03	10.1
Start up (max)	0.72	0.04	2.04	0.06	
RND R/W peak	0.78	0.02	1.96	0.08	
RND R/W average (*2)	0.35	0.02	0.58	0.03	9.9
Standby average	0.13	0.006	0.009	0.001	0.76
Sleep average	0.052	0.005	0.011	0.001	0.39

Figure 49. Power Supply Current of DJNA-371350/370910

(All values in Amps.)	+5Volts		+12Volts		Total (W)
	Pop Mean	Std.Dev	Pop Mean	Std.Dev	
Idle Average	0.25	0.02	0.33	0.03	5.2
Idle ripple (peak-to-peak)	0.25	0.02	0.55	0.07	
Seek peak	0.46	0.02	1.70	0.08	
Seek average (*1)	0.29	0.02	0.50	0.02	7.5
Start up (max)	0.71	0.03	1.94	0.05	
RND R/W peak	0.72	0.03	1.70	0.08	
RND R/W average (*2)	0.35	0.02	0.46	0.02	7.3
Standby average	0.13	0.006	0.009	0.001	0.76
Sleep average	0.052	0.004	0.011	0.001	0.39

Figure 50. Power Supply Current of DJNA-352500/352030

(All values in Amps.)	+5Volts		+12Volts		Total (W)
	Pop Mean	Std.Dev	Pop Mean	Std.Dev	
Idle Average	0.24	0.01	0.26	0.02	4.9
Idle ripple (peak-to-peak)	0.23	0.02	0.50	0.06	
Seek peak	0.46	0.02	1.71	0.06	
Seek average (*1)	0.28	0.01	0.44	0.02	8.9
Start up (max)	0.65	0.03	2.00	0.08	
RND R/W peak	0.70	0.03	1.71	0.06	
RND R/W average (*2)	0.35	0.02	0.4	0.02	8.7
Standby average	0.13	0.006	0.009	0.001	0.76
Sleep average	0.052	0.004	0.011	0.001	0.39

Figure 51. Power Supply Current of DJNA-351520/351010

(All values in Amps.)	+5Volts		+12Volts		Total (W)
	Pop Mean	Std.Dev	Pop Mean	Std.Dev	
Idle Average	0.24	0.01	0.21	0.02	3.4
Idle ripple (peak-to-peak)	0.22	0.01	0.33	0.05	
Seek peak	0.46	0.03	1.56	0.12	
Seek average (*1)	0.28	0.01	0.35	0.02	6.1
Start up (max)	0.64	0.02	1.58	0.17	
RND R/W peak	0.66	0.02	1.56	0.12	
RND R/W average (*2)	0.35	0.01	0.32	0.02	6.2
Standby average	0.13	0.006	0.009	0.001	0.76
Sleep average	0.052	0.004	0.011	0.001	0.39

Notes:

1. Random Seeks at 40% duty cycle.
2. Seek Duty = 30%, W/R Duty = 45%, Idle Duty = 25%.

Figure 52. Power Supply Generated Ripple as seen at file power connector		
	Maximum	**Notes**
+5V DC	100 [mV pp]	0-10 [MHz]
+12V DC	150 [mV pp]	0-10 [MHz]

During file start up and seeking, 12 volt ripple is generated by the file (referred to as dynamic loading). If several files have their power daisy chained together then the power supply ripple plus other file's dynamic loading must remain within the above regulation tolerance. A common supply with separate power leads to each file is a more desirable method of power distribution.

To prevent external electrical noise from interfering with the file's performance, the file must be held by four screws in a user system frame which has no electrical level difference at the four screws position, and has less than +/-300 millivolts peak to peak level difference to the file power connector ground.

6.5.1 Start Up Current

6.5.1.1 DJNA-372200/371800

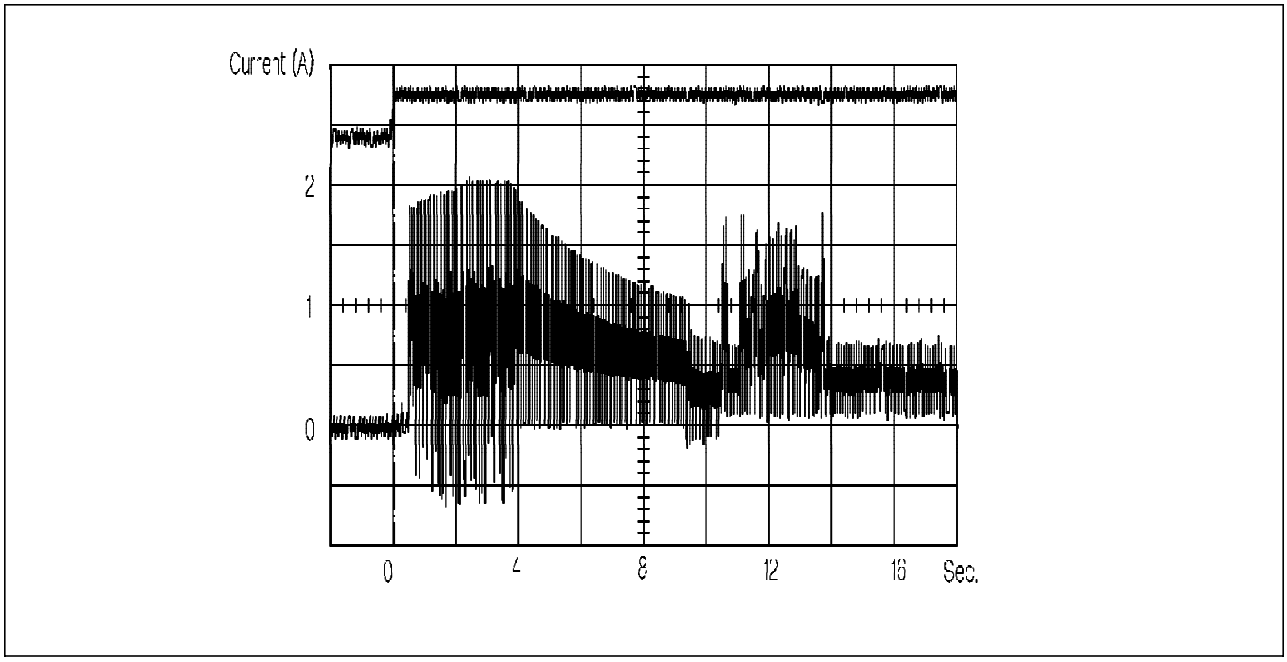


Figure 53. Typical Current Wave Form of 12V at Start Up of DJNA-372200/371800.

6.5.1.2 DJNA-371350/370910

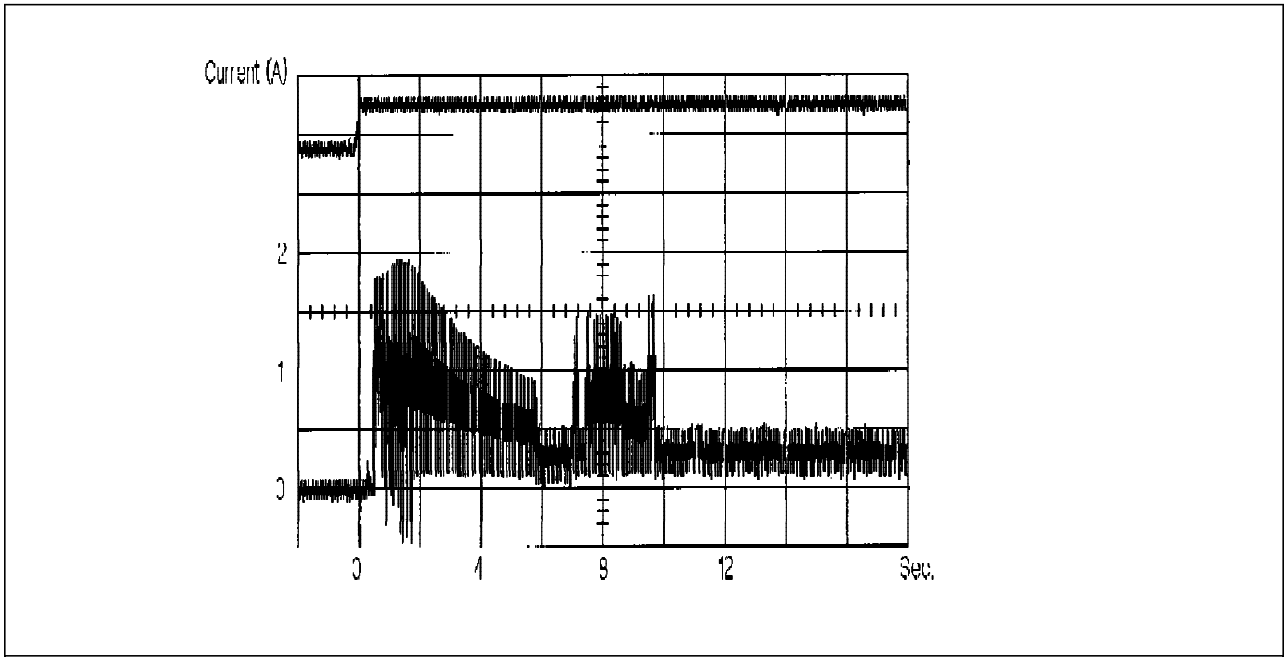


Figure 54. Typical Current Wave Form of 12V at Start Up of DJNA-371350/370910.

6.5.1.3 DJNA-352500/352030

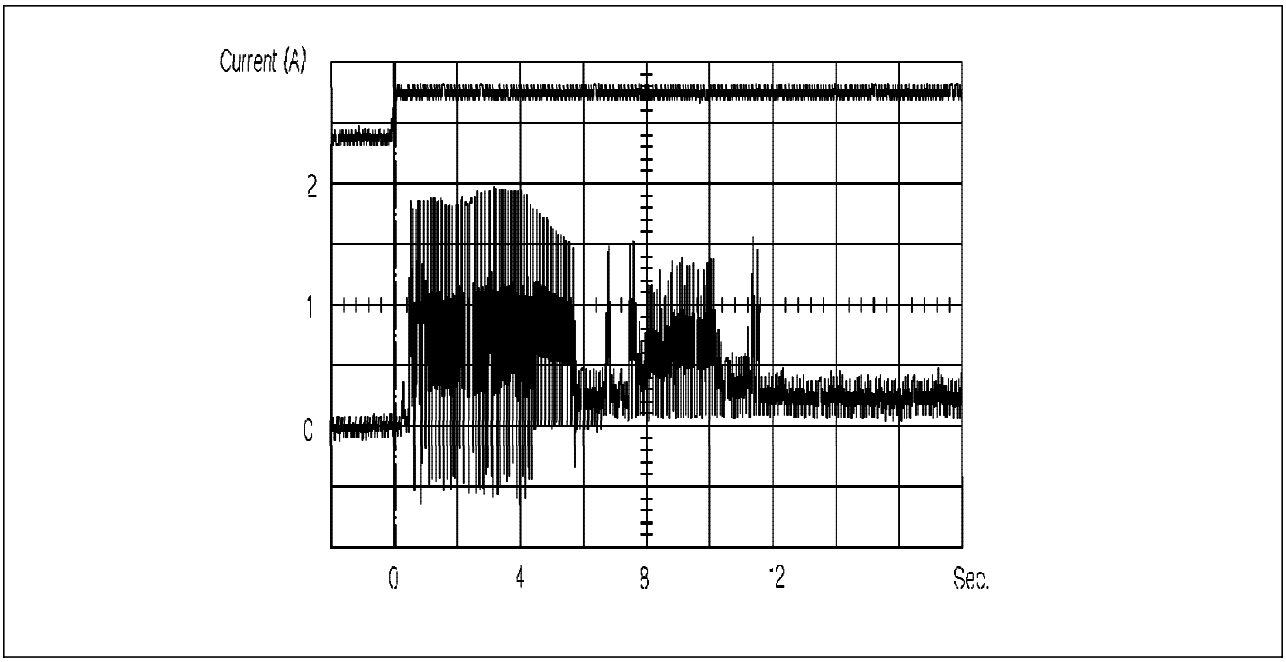


Figure 55. Typical Current Wave Form of 12V at Start Up of DJNA-352500/352030.

6.5.1.4 DJNA-351520/351010

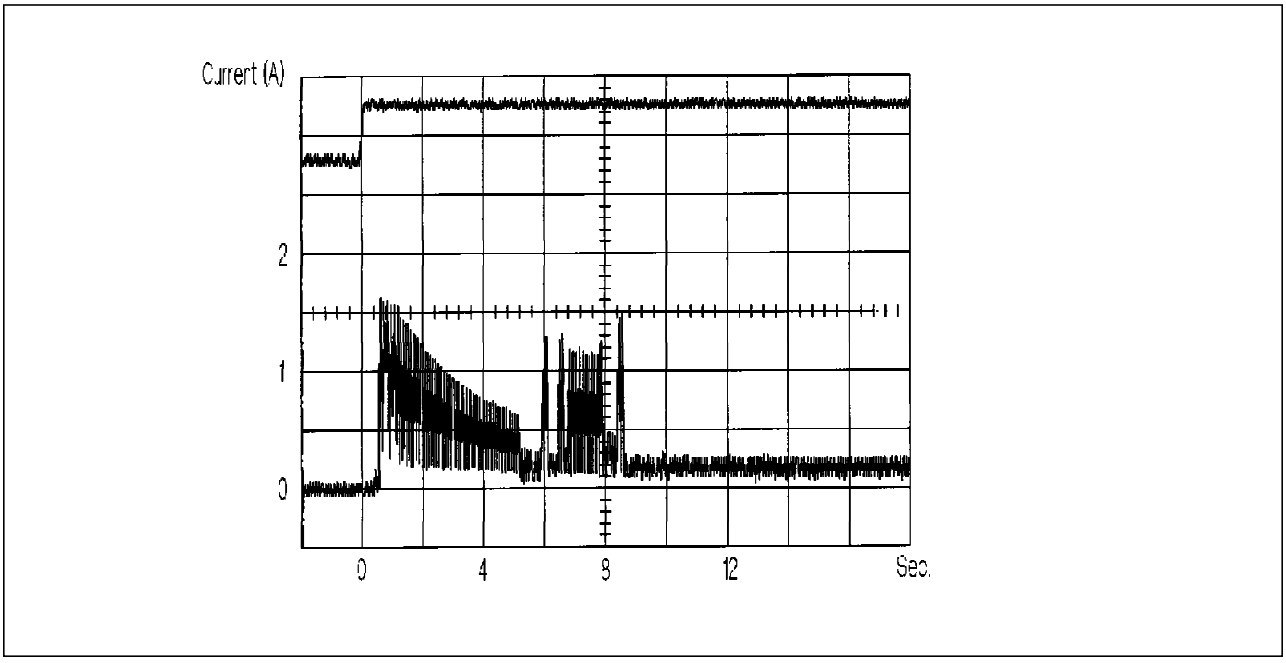


Figure 56. Typical Current Wave Form of 12V at Start Up of DJNA-351520/351010.

6.6 Reliability

6.6.1 Contact Start Stop (CSS)

The drive is designed to withstand a minimum of 40,000 contact start/stop cycles at 40˚C with 13-25% relative humidity.
The drive is designed to withstand a minimum of 10,000 contact start/stop cycles at operating environment conditions specified in 6.4, “Environment” on page 50.

6.6.2 Preventive Maintenance

None.

6.6.3 Data Reliability

- Probability of not recovering data ..... 1 in 10^{13} bits read
- ECC implementation
  On-The-Fly correction, performed as a part of read channel function, recovers up to 12 symbols of error in 1 sector. (1 symbol is 8 bits.)

6.6.4 Cable Noise Interference

To avoid any degradation of performance throughput or error when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

6.7 Mechanical Specifications

6.7.1 Outline

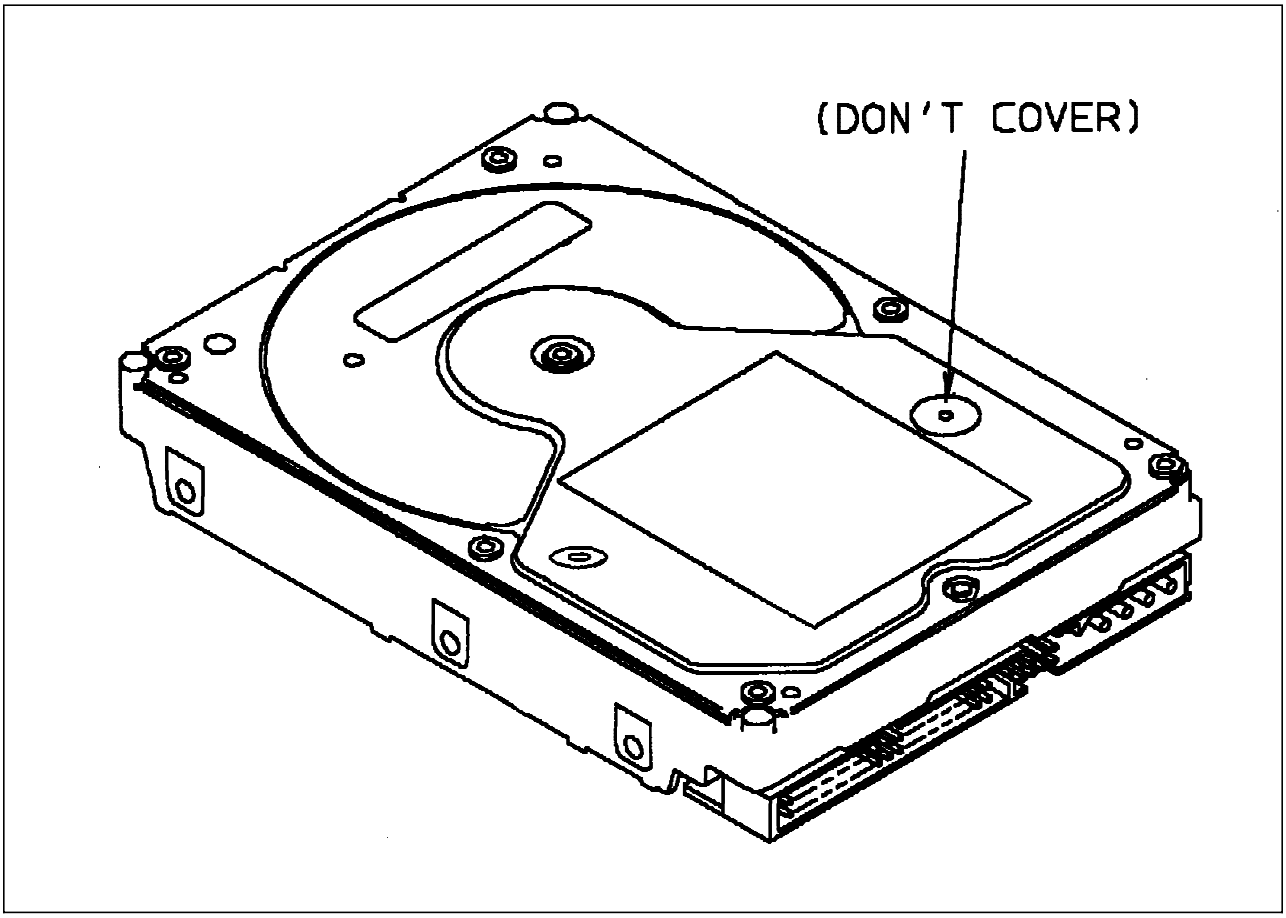


Figure 57. Outline of DJNA-3xxxxx

6.7.2 Mechanical Dimensions and Weight

The following chart describes the dimensions for the 3.5" hard disk drive form factor.

Model	Height (mm)	Width (mm)	Length (mm)	Weight (gram)
DJNA-372200/371800	25.4 ± 0.4	101.6 ± 0.4	146.0 ± 0.6	630 Max
DJNA-352500/352030	25.4 ± 0.4	101.6 ± 0.4	146.0 ± 0.6	630 Max
DJNA-371350/370910	25.4 ± 0.4	101.6 ± 0.4	146.0 ± 0.6	560 Max
DJNA-351520/351010	25.4 ± 0.4	101.6 ± 0.4	146.0 ± 0.6	560 Max

Figure 58. Physical Dimension and Weight

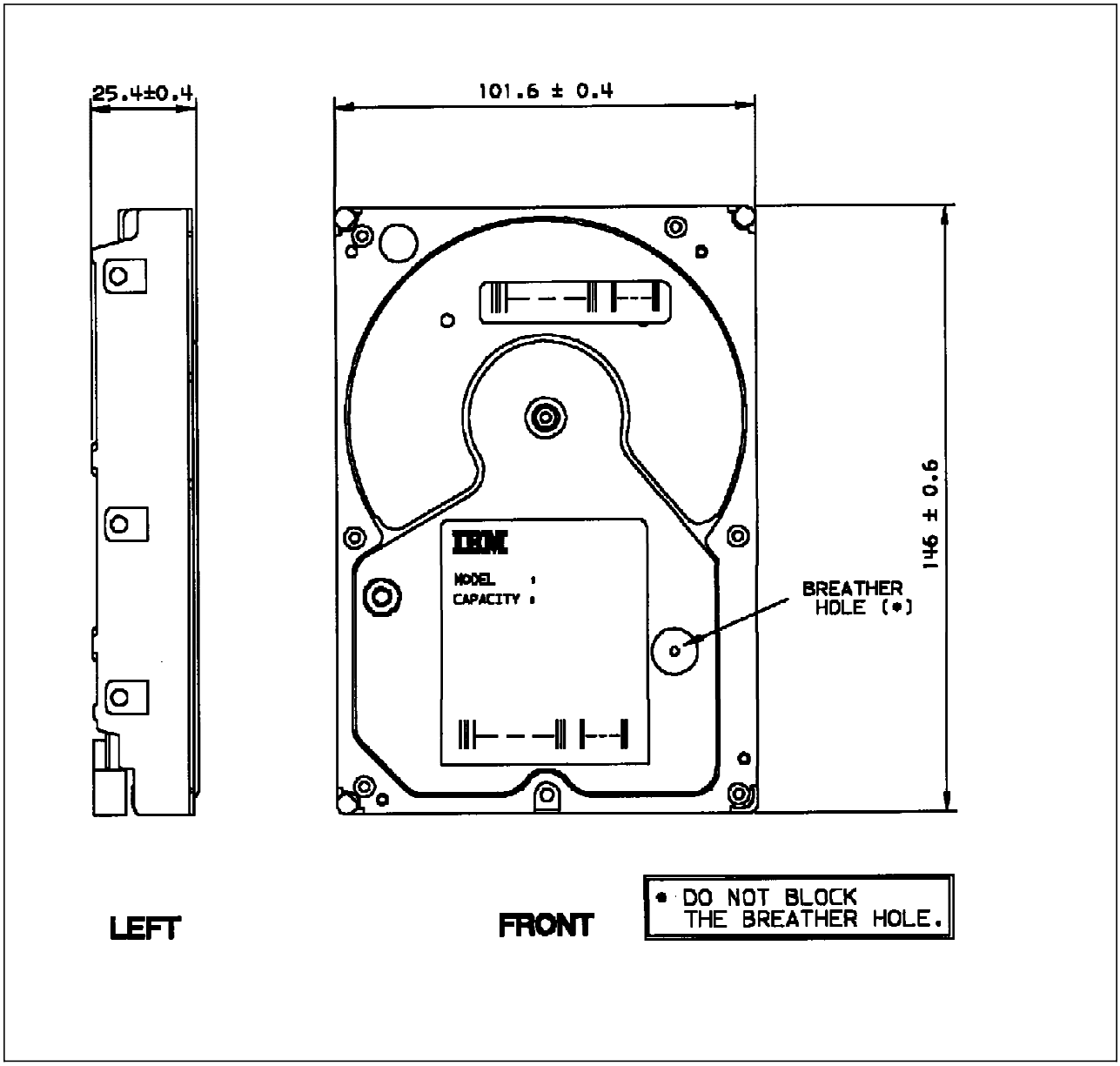


Figure 59. Mechanical Dimension

6.7.3 Connector Locations

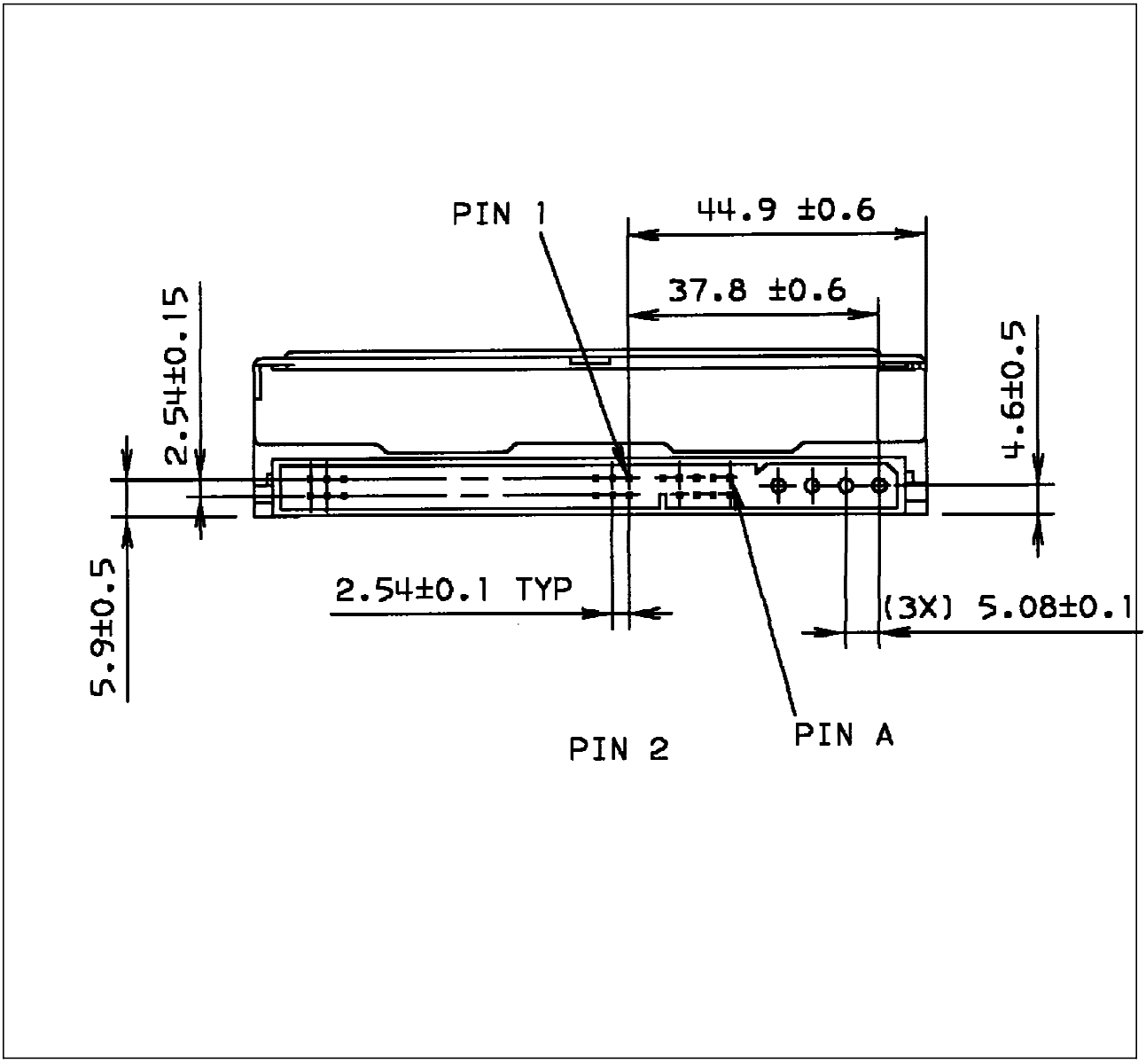


Figure 60. Connector Locations

6.7.4 Hole Locations

The Figure 61 on page 60 shows the outline of DJNA-3xxxxx which includes the hole locations.

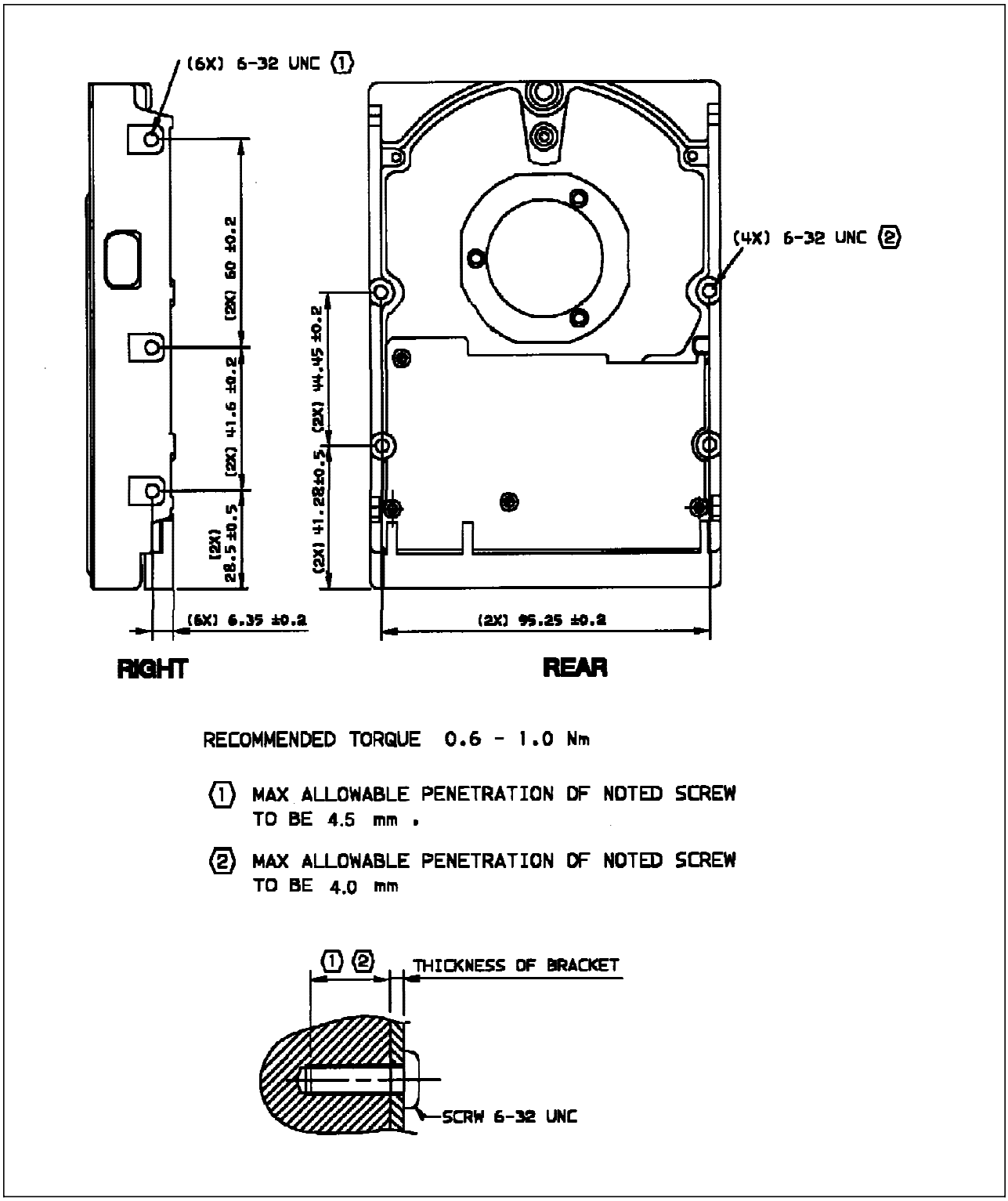


Figure 61. Mounting Positions and the Tappings

6.7.5 Mounting Orientation

The drive will operate in all axes (6 directions). The drive will operate within the specified error rates when tilted ± 5 degree from these positions.

Performance and error rate will stay within specification limits if the drive is operated in the other permissible orientations from which it was formatted. Thus a drive formatted in a horizontal orientation will be able to run vertically and vice versa.

The recommended mounting **screw torque** is **0.6 - 1.0** [Nm] (6 - 10 [Kgf.cm]).
The recommended mounting screw depth is 4 [mm] Max for bottom and 4.5 [mm] Max for horizontal mounting.

In case electrical screw driver is used for mounting screws, **Current Control Type Electrical Screw Driver** should be used.
Mechnical Latch Type Electrical Screw Driver is not recommended because of possibility of mechanical shock higher than specification value which may cause HDD damage.

The system is responsible for mounting the drive securely enough to prevent from excessive motion or vibration of the drive at seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware.

Vibration test and shock test are to be conducted by mounting the drive to the table using bottom four screws.

6.7.6 Shipping Zone and Lock

A "shipping" (or "landing") zone on the disk, not on the data area of the disk, is provided to protect the disk data during shipping, movement, or storage. Upon power down, a head locking mechanism will secure the heads in this zone. See Non-Operating Shock section for additional details.

6.8 Vibration and Shock

All vibration and shock measurements in this section are made with the drive that has no mounting attachments for the systems. The input power for the measurements is applied to the normal drive mounting points.

6.8.1 Operating Vibration

6.8.1.1 Random Vibration

The drive is designed to operate without unrecoverable errors while being subjected to the following vibration levels.

The measurements are carried out during 30 minutes of random vibration using the power spectral density (PSD) levels as following.

Figure 62. Random Vibration PSD Profile Breakpoints (Operating)

	Random Vibration PSD Profile Breakpoints (Operating)								
[Hz]	5	17	45	48	62	65	150	200	500
Holizontal vibration $\times 10^{-3}$ [G^2/Hz]	0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.5	0.5
Vertical vibration $\times 10^{-3}$ [G^2/Hz]	0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.08	0.08

Overall RMS (root mean square) level of holizontal vibration is 0.67G RMS.
Overall RMS (root mean square) level of vertical vibration is 0.56G RMS.

Note: The specified levels are measured at the mounting points.

6.8.1.2 Swept Sine Vibration

The hard disk drive will meet the criteria shown below while operating in respective conditions.

No errors 0.5 G 0-peak, 5-300-5 Hz sine wave, 0.5 oct/min sweep rate with 3 minutes dwells at 2 major resonances

No data loss 1 G 0-peak, 5-300-5 Hz sine wave, 0.5 oct/min sweep rate with 3 minutes dwells at 2 major resonances

6.8.2 Non-Operating Vibrations

The drive does not sustain permanent damage or loss of recorded data after being subjected to the environment described below.

6.8.2.1 Random Vibration

The test consists of a random vibration applied for each of three mutually perpendicular axes with the time duration of 10 minutes per axis. The PSD levels for the test simulates the shipping and relocation environment which is shown below.

Figure 63. Random Vibration PSD Profile Breakpoints (Non-Operating)

	Random Vibration PSD Profile Breakpoints (Non-Operating)						
Hz	2	4	8	40	55	70	200
[G^2/Hz]	0.001	0.03	0.03	0.003	0.01	0.01	0.001

Overall RMS (Root Mean Square) level of vibration is 1.04G (RMS).

6.8.2.2 Swept Sine Vibration

- 2 G (Zero to peak), 5 to 500 to 5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwell at two major resonances

6.8.3 Operating Shock

The drive meets the following criteria.

- No data loss with 10G 11msec half-sine shock pulse
- No data loss with 65G 2msec half-sine shock pulse

The shock pulses of each level are applied to the drive, ten pulses for each direction and for all three axes. There must be a minimum of 30 seconds delay between shock pulses. The input level is applied to a base plate where the drive is attached with four screws.

6.8.4 Non-Operating Shock

The drive withstands the following half-sine shock pulse

- No data loss with 75G 11ms
- No data loss with 175G 2ms

The shocks are applied for each direction of the drive for three mutually perpendicular axes and one axis at a time. Input levels are measured on a base plate where the drive is attached with four screws.

6.8.4.1 Rotational Shock

The drive withstands the following Non-Operating Rotational Shock.

DJNA-352500/352030/372200/371800

- No data loss with Rotational Shock 25,000 rad/s² 1ms applied around the axis of actuator pivot.
- No data loss with Rotational Shock 15,000 rad/s² 2ms applied around the axis of actuator pivot.

DJNA-351520/351010/371350/370910

- No data loss with Rotational Shock 25,000 rad/s² 1ms applied around the axis of actuator pivot.
- No data loss with Rotational Shock 18,000 rad/s² 2ms applied around the axis of actuator pivot.

Note: Actuator is automatically locked at power-off to keep the heads on a landing zone.

6.9 Acoustics

The following shows the acoustic levels.

6.9.1 Sound Power Levels

The upper limit criteria of the A-weighted sound power levels are given in Bel relative to one pico watt and are shown in the following table. The measurment method is in accodance with ISO7779.

Figure 64. Sound Power Levels of DJNA-35xxxx

Mode	**A-weighted Sound Power Level [Bel]**
Idle	3.5 (Typical) 3.8 (Max)
Operating	4.2 (Typical) 4.5 (Max)

Figure 65. Sound Power Levels of DJNA-37xxxx

Mode	**A-weighted Sound Power Level [Bel]**
Idle	3.8 (Typical) 4.2 (Max)
Operating	4.5 (Typical) 4.8 (Max)

Background power levels of the acoustic test chamber for each octave band are to be recorded.
Sound power levels are measured with the drive supported by spacers so that the lower surface of the drive is located 25 ± 3mm height from the chamber desk. No sound absorbing material shall be used.
The acoustical characteristics of the drive subsystem are measured under the following conditions.

Idle mode:

Powered on, disks spinning, track following, unit ready to receive and respond to control line commands.

Operating mode:

Continuous random cylinder selection and seek operation of actuator with a delay for a time period achieving the required seek rate Ns according to the following formula:

$$Ns = 0.4 / (Tt + Tl)$$

where:

Ns = average seek rate in seeks/sec.
Tt = published random seek time.
Tl = time for the drive to rotate by half a revolution.

6.9.2 Sound Pressure (Reference)

6.9.2.1 Unit Sound Pressure Level Measurment

The hard disk drives are measured in a semi-anechoic chamber, with background noise = < 25 dBA. Surfaces to be measured are top cover side and card side. Microphone is set one meter above the drive surface.

Random operation mode is simulated with 40% seek and 60% idle in time.

6.9.2.2 Sound Pressure Level

The hard disk drives meet the following sound pressure level.

Figure 66. Sound Pressure Level of DJNA-35xxxx

Mode	Mean	Max
Idle on Track	33 dBA	37 dBA
Random Operation	38 dBA	41 dBA

Figure 67. Sound Pressure Level of DJNA-37xxxx

Mode	Mean	Max
Idle on Track	34 dBA	38 dBA
Random Operation	39 dBA	42 dBA

6.10 Identification

6.10.1 Labels

The following labels are affixed to every disk drive .

1. A label containing IBM logo, IBM part number and the statement 'Made by IBM' or equivalent.
2. A label containing drive model number, date code, formatted capacity, place of manufacture, and UL/CSA/TUV/CE/C-Tick mark logos.
3. A bar code label containing the drive serial number.
4. A label containing jumper pin description.

The labels may be integrated with other labels.

6.11 Electromagnetic Compatibility

The drive, when installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate, shall meet the worldwide EMC requirements listed below.

IBM will provide technical support to assist users in complying with the EMC requirements.

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15.
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP).

6.11.1 CE Mark

The DJNA-3xxxxx complies with EC directive 89/336/EEC. CE mark for the certification is indicated on the drive label.

6.11.2 C-Tick Mark

The DJNA-3xxxxx complies with the following Australian EMC standard.

- Limits and methods of measurement of radio disturbance characteristics of information technology equipment, AS/NZS 3548:1995 CLASS-B.

6.12 Safety

6.12.1 Underwriters Lab(UL) Approval

DJNA-3xxxxx complies with UL 1950.

6.12.2 Canadian Standards Authority(CSA) Approval

DJNA-3xxxxx complies with CAN/CSA-22.2 No.0-M1989 and No.950-M1995.

6.12.3 IEC Compliance

DJNA-3xxxxx complies with IEC 950.

6.12.4 German Safety Mark

DJNA-3xxxxx are approved by TUV on Test Requirement: EN 60 950:1992/A1-4.

6.12.5 Flammability

Printed Circuit boards used in this product are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better except minor mechanical parts.

6.12.6 Secondary Circuit Protection

Fuses are provided in 12V input of the hard disk drive for over current protection.

6.13 Packaging

Drives are shipped in ESD protective bags.

Part 2. ATA Interface Specification

7.0 General

7.1 Introduction

This specification describes the host interface to DJNA-3xxxxx.

The interface conforms to the Working Document of Information technology - AT Attachment with Packet Interface Extension (ATA/ATAPI-4) Revision 17 dated on 30 October 1997 with certain limitations described in 8.0, “Deviations From Standard” on page 73.

In addition to the above, DJNA-3xxxxx supports also Ultra DMA Mode-4 (Ultra ATA/66).

7.2 Terminology

Device Device indicates DJNA-3xxxxx.

Host Host indicates the system that the device is attached to.

8.0 Deviations From Standard

The device conforms to the referenced specifications, with deviations described below.

Check Power Mode Check Power Mode command returns FFh to Sector Count Register when the device is in Idle mode. This command does not support 80h as the return value.

Hard Reset Hard reset response is not the same as that of power on reset. Refer to section 10.1, “Reset Response” on page 81 for detail.

9.0 Registers

Addresses					Functions	
CS0–	CS1–	DA2	DA1	DA0	READ(DIOR–)	WRITE(DIOW–)
N	N	x	x	x	Data bus high imped*1	Not used
					Control block registers	
N	A	0	x	x	Data bus high imped*1	Not used
N	A	1	0	x	Data bus high imped*1	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	Device Address	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error Register	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	0	1	1	*2 LBA bits 0– 7	*2 LBA bits 0– 7
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	0	*2 LBA bits 8–15	*2 LBA bits 8–15
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	0	1	*2 LBA bits 16–23	*2 LBA bits 16–23
A	N	1	1	0	Device/Head	Device/Head
A	N	1	1	0	*2 LBA bits 24–27	*2 LBA bits 24–27
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

*1 "imped" stands for "impedance".
*2 Mapping of registers in LBA mode

Logic conventions : A = signal asserted
N = signal negated
x = does not matter which it is

Figure 68. Register Set

Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA2, DA1, DA0, DIOR- and DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device.

The Control Block Registers are used for device control and to post alternate status.

9.1 Alternate Status Register

Alternate Status Register							
7 BSY	6 RDY	5 DF	4 DSC /SERV	3 DRQ	2 COR	1 IDX	0 ERR

Figure 69. Alternate Status Register

This register contains the same information as the Status Register. The only difference is that reading this register does not imply interrupt acknowledge or clear a pending interrupt. See 9.13, “Status Register” on page 79 for the definition of the bits in this register.

9.2 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in Figure 85 on page 107.

All other registers required for the command must be set up before writing the Command Register.

9.3 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16-23. At the end of the command, this register is updated to reflect the current LBA Bits 16-23.

The cylinder number may be from zero to the number of cylinders minus one.

9.4 Cylinder Low Register

This register contains the low order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8-15. At the end of the command, this register is updated to reflect the current LBA Bits 8-15.

The cylinder number may be from zero to the number of cylinders minus one.

9.5 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command, and configuration information is transferred on an Identify Device command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ=1 in the Status Register.

9.6 Device Control Register

Device Control Register							
7	6	5	4	3	2	1	0
—	—	—	—	1	SRST	—IEN	0

Figure 70. Device Control Register

Bit Definitions

SRST (RST) Software Reset. The device is held reset when RST=1. Setting RST=0 re-enables the device.

The host must set RST=1 and wait for at least 5 microseconds before setting RST=0, to ensure that the device recognizes the reset.

-IEN Interrupt Enable. When -IEN=0, and the device is selected, device interrupts to the host will be enabled. When -IEN=1, or the device is not selected, device interrupts to the host will be disabled.

9.7 Drive Address Register

Drive Address Register							
7	6	5	4	3	2	1	0
HIZ	—WTG	—H3	—H2	—H1	—H0	—DS1	—DS0

Figure 71. Drive Address Register

This register contains the inverted drive select and head select addresses of the currently selected drive.

Bit Definitions

HIZ High Impedance. This bit is not drived and will always be in a high impedance state.

-WTG -Write Gate. This bit is 0 when writing to the disk device is in progress.

-H3,-H2,-H1,-H0 -Head Select. These four bits are the one's complement of the binary coded address of the currently selected head. -H0 is the least significant.

-DS1 -Drive Select 1. Drive select bit for device 1, active low. DS1=0 when device 1 (slave) is selected and active.

-DS0 -Drive Select 0. Drive select bit for device 0, active low. DS0=0 when device 0 (master) is selected and active.

9.8 Device/Head Register

Device/Head Register							
7 1	6 L	5 1	4 DRV	3 HS3	2 HS2	1 HS1	0 HS0

Figure 72. Device/Head Register

This register contains the device and head numbers.

Bit Definitions

L Binary encoded address mode select. When L=0, addressing is by CHS mode. When L=1, addressing is by LBA mode.

DRV Device. When DRV=0, device 0 (master) is selected. When DRV=1, device 1 (slave) is selected.

HS3,HS2,HS1,HS0 Head Select. These four bits indicate binary encoded address of the head. HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head.

The head number may be from zero to the number of heads minus one.

In LBA mode, HS3 through HS0 contain bits 24-27 of the LBA. At command completion, these bits are updated to reflect the current LBA bits 24-27.

9.9 Error Register

Error Register							
7 ICRCE	6 UNC	5 0	4 IDNF	3 0	2 ABRT	1 TK0NF	0 AMNF

Figure 73. Error Register

This register contains status from the last command executed by the device, or a diagnostic code.

At the completion of any command except Execute Device Diagnostic, the contents of this register are valid always even if ERR=0 in the Status Register.

Following a power on, a reset, or completion of an Execute Device Diagnostic command, this register contains a diagnostic code. See Figure 77 on page 82 for the definition.

Bit Definitions

ICRCE (CRC) Interface CRC Error. CRC=1 indicates a CRC error has occurred on the data bus during a Ultra-DMA transfer.

UNC Uncorrectable Data Error. UNC=1 indicates an uncorrectable data error has been encountered.

IDNF (IDN) ID Not Found. IDN=1 indicates the requested sector's ID field could not be found.

ABRT (ABT) Aborted Command. ABT=1 indicates the requested command has been aborted due to a device status error or an invalid parameter in an output register.

TK0NF (T0N) Track 0 Not Found. T0N=1 indicates track 0 was not found during a Recalibrate command.

AMNF (AMN) Address Mark Not Found. AMN=1 indicates the data address mark has not been found after finding the correct ID field for the requested sector.

9.10 Features Register

This register is command specific. This is used with the Set Features command and S.M.A.R.T. Function Set command.

9.11 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors is specified.

If the register is zero at command completion, the command was successful. If not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

9.12 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode, this register contains Bits 0-7. At the end of the command, this register is updated to reflect the current LBA Bits 0-7.

9.13 Status Register

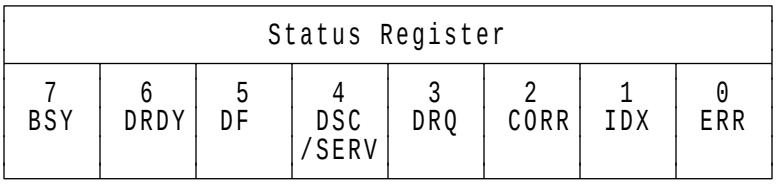


Figure 74. Status Register

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

The use of bit 4 is command dependent. After the DMA Queued commands, it is used as SERV. After any other commands or reset, it is used as DSC.

Bit Definitions

BSY Busy. BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.

DRDY (RDY) Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to 0 during power on until the device is ready to accept a command. If the device detects an error while processing a command, RDY is set to 0 until the Status Register is read by the host, at which time RDY is set back to 1.

DF Device Fault. DF=1 indicates that the device has detected a write fault condition. DF is set to 0 after the Status Register is read by the host.

DSC Device Seek Complete. DSC=1 indicates that a seek has completed and the device head is settled over a track. DSC is set to 0 by the device just before a seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host, at which time the bit again indicates the current seek complete status.

When the device enters into or is in Standby mode or Sleep mode, this bit is set by device in spite of not spinning up.

SERV (SRV) Service. SRV is set to one when the device is ready to transfer data after it releases bus for execution of a DMA Queued command.

DRQ Data Request. DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.

CORR (COR) Corrected Data. Always 0.

IDX Index. IDX=1 once per revolution. Since IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is reading the Status Register continuously. Therefore the host should not attempt to use IDX for timing purposes.

ERR Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets ERR=0 when the next command is received from the host.

10.0 General Operation Descriptions

10.1 Reset Response

There are three types of reset in ATA as follows:

Power On Reset (POR)

The device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametrics, and sets default values.

Hard Reset (Hardware Reset) RESET- signal is negated in ATA Bus.

The device resets the interface circuitry as well as Soft Reset.

Soft Reset (Software Reset) SRST bit in the Device Control Register is set, then is reset.

The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset is shown in Figure 75

	POR	hard reset	soft reset
Aborting Host interface	—	o	o
Aborting Device operation	—	(*1)	(*1)
Initialization of hardware	o	x	x
Internal diagnostic	o	x	x
Spinning spindle	o	x	x
Initialization of registers (*2)	o	o	o
DASP handshake	o	o	x
PDIAG handshake	o	o	o
Reverting programmed parameters to default	o	(*3)	(*3)
– Number of CHS (set by Initialize Device Parameter)			
– Multiple mode			
– Write cache			
– Read look–ahead			
– ECC bytes			
Disable Standby timer	o	x	x
Power mode	Idle	(*4)	(*4)

o — execute
x — not execute

Figure 75. Reset Response Table

Note.

(*1) Execute after the data in write cache has been written.

(*2) Default value on POR is shown in Figure 76 on page 82.

(*3) The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.

(*4) In the case of Sleep mode, the device goes to Standby mode. In other case, the device does not change current mode.

10.1.1 Register Initialization

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	A0h
Status	50h
Alternate Status	50h

Figure 76. Default Register Values

After power on, hard reset, or software reset, the register values are initialized as shown in Figure 76.

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Device 1 failed

Figure 77. Diagnostic Codes

The meaning of the Error Register diagnostic codes resulting from power on, hard reset or the Execute Device Diagnostic command are shown in Figure 77.

10.2 Diagnostic and Reset considerations

For each Reset and Execute Device Diagnostic, the diagnostic is done as follows:

Power On Reset

DASP- is read by Device 0 to determine if Device 1 is present. If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has powered on or reset without error, otherwise Device 0 clears

the BSY bit whenever it is ready to accept commands. Device 0 may assert DASP- to indicate device activity.

Hard Reset, Soft Reset

If Device 1 is present Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and whether Device 1 has reset without any errors, otherwise Device 0 shall simply reset and clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

Execute Device Diagnostic

If Device 1 is present, Device 0 shall read PDIAG- to determine when it is valid to clear the BSY bit and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTIC command, otherwise Device 0 shall simply execute its diagnostics and then clear the BSY bit. DASP- is asserted by Device 0 (and Device 1 if it is present) in order to indicate the device is active.

In all the above cases: Power on, RESET-, Soft reset, and the EXECUTE DEVICE DIAGNOSTIC command the Device 0 Error register is shown in Figure 78.

Device 1 Present?	PDIAG– Asserted?	Device 0 Passed	Error Register
Yes	Yes	Yes	01h
Yes	Yes	No	0xh
Yes	No	Yes	81h
Yes	No	No	8xh
No	(not read)	Yes	01h
No	(not read)	No	0xh

Where x indicates the appropriate Diagnostic Code for the Power on, RESET-, Soft reset, or Device Diagnostic error.

Figure 78. Reset error register values

10.3 Sector Addressing Mode

All addressing of data sectors recorded on the device's media is by a logical sector address. The logical CHS address for DJNA-3xxxxx is different from the actual physical CHS location of the data sector on the disk media.

DJNA-3xxxxx support both Logical CHS Addressing Mode and LBA Addressing Mode as the sector addressing mode.

The host system may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the DEVICE/HEAD register. So a host system must set the L bit to 1 if the host uses LBA Addressing mode.

10.3.1 Logical CHS Addressing Mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but can not exceed 255(0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode buf can not exceed 15(0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65535(0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

The default CHS translation mode is described in the Identify Device Information. The current CHS translation mode also is described in the Identify Device Information.

10.3.2 LBA Addressing Mode

Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following is always true:

```
LBA = (  (cylinder * heads_per_cylinder + heads)
       * sectors_per_track ) + sector - 1


where heads_per_cylinder and sectors_per_track
are the current translation mode values.
```

On LBA addressing mode, the LBA value is set to the following register.

```
Device/Head      <---   LBA bits 27-24
Cylinder High    <---   LBA bits 23-16
Cylinder Low     <---   LBA bits 15- 8
Sector Number    <---   LBA bits  7- 0
```

10.4 Overlapped and Queued Feature

Overlap allows devices to perform a bus release so that the other device on the bus may be used. To perform a bus release the device clears both DRQ and BSY to zero. When selecting the other device during overlapped operations, the host shall disable interrupts via the nIEN bit on the currently selected device before writing the Device/Head register to select the other device.

The only commands that may be overlapped are:

NOP (with 01h subcommand code)	('00'h)
Read DMA Queued	('C7'h)
Service	('A2'h)
Write DMA Queued	('CC'h)

For the READ DMA QUEUED and WRITE DMA QUEUED commands, the device may or may not perform a bus release. If the device is ready to complete execution of the command, it may complete the command immediately. If the device is not ready to complete execution of the command, the device may perform a bus release and complete the command via a service request.

Command queuing allows the host to issue concurrent commands to the same device. Only commands included in the overlapped feature set may be queued. If a queue exists when a non-queued command is received, the non-queued command shall be aborted and the commands in the queue shall be discarded. The ending status shall be ABORT command and the results are indeterminant.

The maximum queue depth supported by a device is indicated in word 73 of the Identify Device information.

A queued command shall have a Tag provided by the host in the Sector Count register to uniquely identify the command. When the device restores register parameters during the execution of the SERVICE command, this Tag shall be restored so that the host may identify the command for which status is being presented. If a queued command is issued with a Tag value that is identical to the Tag value for a command already in the queue, the entire queue is aborted including the new command. The ending status is ABORT command and the results are indeterminant. If any error occurs, the command queue is aborted.

When the device is ready to continue the processing of a bus released command and BSY and DRQ are both cleared to zero, the device requests service by setting SERV to one, setting a pending interrupt, and asserting INTRQ if selected and if nIEN is cleared to zero. SERV shall remain set until all commands ready for service have been serviced. The pending interrupt shall be cleared and INTRQ negated by a Status register read or a write to the Command register.

When the device is ready to continue the processing of a bus released command and BSY or DRQ is set to one (i.e., the device is processing another command on the bus), the device requests service by setting SERV to one. SERV shall remain set until all commands ready for service have been serviced. At command completion of the current command processing (i.e., when both BSY and DRQ are cleared to zero), the device shall process interrupt pending and INTRQ per the protocol for the command being completed. No additional interrupt shall occur due to other commands ready for service until after the device's SERV bit has been cleared to zero.

When the device receives a new command while queued commands are ready for service, the device shall execute the new command and process interrupt pending and INTRQ per the protocol for the new command. If the queued commands ready for service still exist at command completion of this command, SERV remains set to one but no additional interrupt shall occur due to commands ready for service.

When queuing commands, the host shall disable interrupts via the nIEN bit before writing a new command to the Command register and may re-enable interrupts after writing the command. When reading status at command completion of a command, the host shall check the SERV bit since the SERV bit may be set because the device is ready for service associated with another queued command. The host receives no additional interrupt to indicate that a queued command is ready for service.

10.5 Power Management Feature

The power management feature set permits a host to modify the behavior of a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enable a device to implement low power consumption modes.

DJNA-3xxxxx implement the following set of functions.

1. A Standby timer

2. Idle command
3. Idle Immediate command
4. Sleep command
5. Standby command
6. Standby Immediate command

10.5.1 Power Mode

The lowest power consumption when the device is powered on occurs in Sleep Mode. When in sleep mode, the device requires a reset to be activated.

In Standby Mode the device interface is capable of accepting commands, but as the media may not immediately accessible, there is a delay while waiting for the spindle to reach operating speed.

In Idle Mode the device is capable of responding immediately to media access requests.

In Active Mode the device is under executing a command or accessing the disk media with read look-ahead function or write cache function.

10.5.2 Power Management Commands

The Check Power Mode command allows a host to determine if a device is currently in, going to or leaving standby mode.

The Idle and Idle Immediate commands move a device to idle mode immediately from the active or standby modes. The idle command also sets the standby timer count and starts the standby timer.

The Standby and Standby Immediate commands move a device to standby mode immediately from the active or idle modes. The standby command also sets the standby timer count.

The Sleep command moves a device to sleep mode. The device's interface becomes inactive at the completion of the sleep command. A reset is required to move a device out of sleep mode. When a device exits sleep mode it will enter Standby mode.

10.5.3 Standby timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the standby mode.

If the value of SECTOR COUNT register on Idle command or Standby command is set to 00h, the standby timer is disabled.

10.5.4 Interface Capability for Power Modes

The each power mode affects the physical interface as defined in the following table:

Mode	BSY	RDY	Interface active	Media
Active	x	x	Yes	Active
Idle	0	1	Yes	Active
Standby	0	1	Yes	Inactive
Sleep	0	1	No	Inactive

Figure 79. Power conditions

Ready(RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

10.6 S.M.A.R.T. Function

The intent of Self-monitoring, analysis and reporting technology (S.M.A.R.T) is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

10.6.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

10.6.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. The valid range of attribute values is from 1 to 253 decimal. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or faulty condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or faulty condition existing.

10.6.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical value of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimal.

10.6.4 Threshold exceeded condition

If one or more attribute values, whose Pre-failure bit of their status flag is set, are less than or equal to their corresponding attribute thresholds, then the device reliability status is negative, indicating an impending degrading or faulty condition.

10.6.5 S.M.A.R.T. commands

The S.M.A.R.T. commands provide access to attribute values, attribute thresholds and other logging and reporting information.

10.7 Security Mode Feature Set

Security Mode Feature Set is a powerful security feature. With a device lock password, a user can prevent unauthorized access to hard disk device even if the device is removed from the computer.

The following commands are supported for this feature.

Security Set Password	('F1'h)
Security Unlock	('F2'h)
Security Erase Prepare	('F3'h)
Security Erase Unit	('F4'h)
Security Freeze Lock	('F5'h)
Security Disable Password	('F6'h)

10.7.1 Security mode

Following security modes are provided.

Device Locked mode The device disables media access commands after power on. Media access commands are enabled by either a security unlock command or a security erase unit command.

Device Unlocked mode The device enables all commands. If a password is not set this mode is entered after power on, otherwise it is entered by a security unlock or a security erase unit command.

Device Frozen mode The device enables all commands except those which can update the device lock function, set/change password. The device enters this mode via a Security Freeze Lock command. It cannot quit this mode until power off.

10.7.2 Security level

Following security levels are provided.

High level security When the device lock function is enabled and the User Password is forgotten the device can be unlocked via a Master Password.

Maximum level security When the device lock function is enabled and the User Password is forgotten then only the Master Password with a Security Erase Unit command can unlock the device. Then user data is erased.

10.7.3 Password

This function can have 2 types of passwords as described below.

Master Password When the Master Password is set, the device does NOT enable the Device Lock Function, and the device can NOT be locked with the Master Password, but the Master Password can be used for unlocking the device locked.

User Password The User Password should be given or changed by a system user. When the User Password is set, the device enables the Device Lock Function, and then the device is locked on next power on reset or hard reset.

The system manufacturer/dealer who intends to enable the device lock function for the end users, must set the master password even if only single level password protection is required.

10.7.4 Operation example

10.7.4.1 Master Password setting

The system manufacturer/dealer can set a new Master Password from default Master Password using the Security Set Password command, without enabling the Device Lock Function.

10.7.4.2 User Password setting

When a User Password is set, the device will automatically enter lock mode the next time the device is powered on.

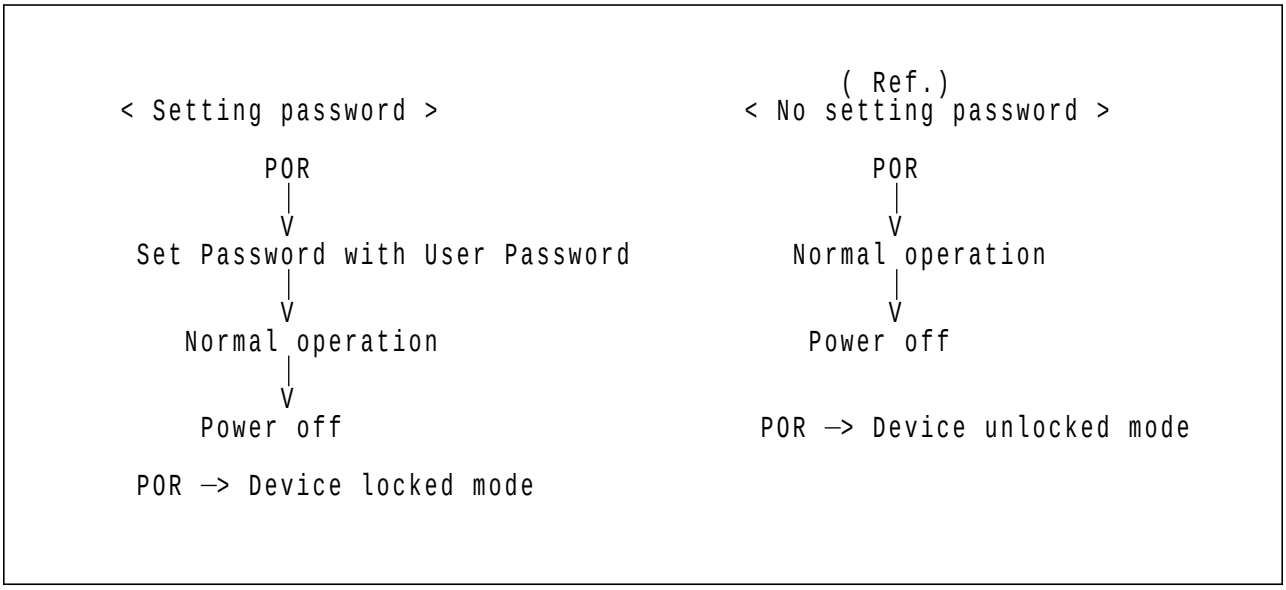
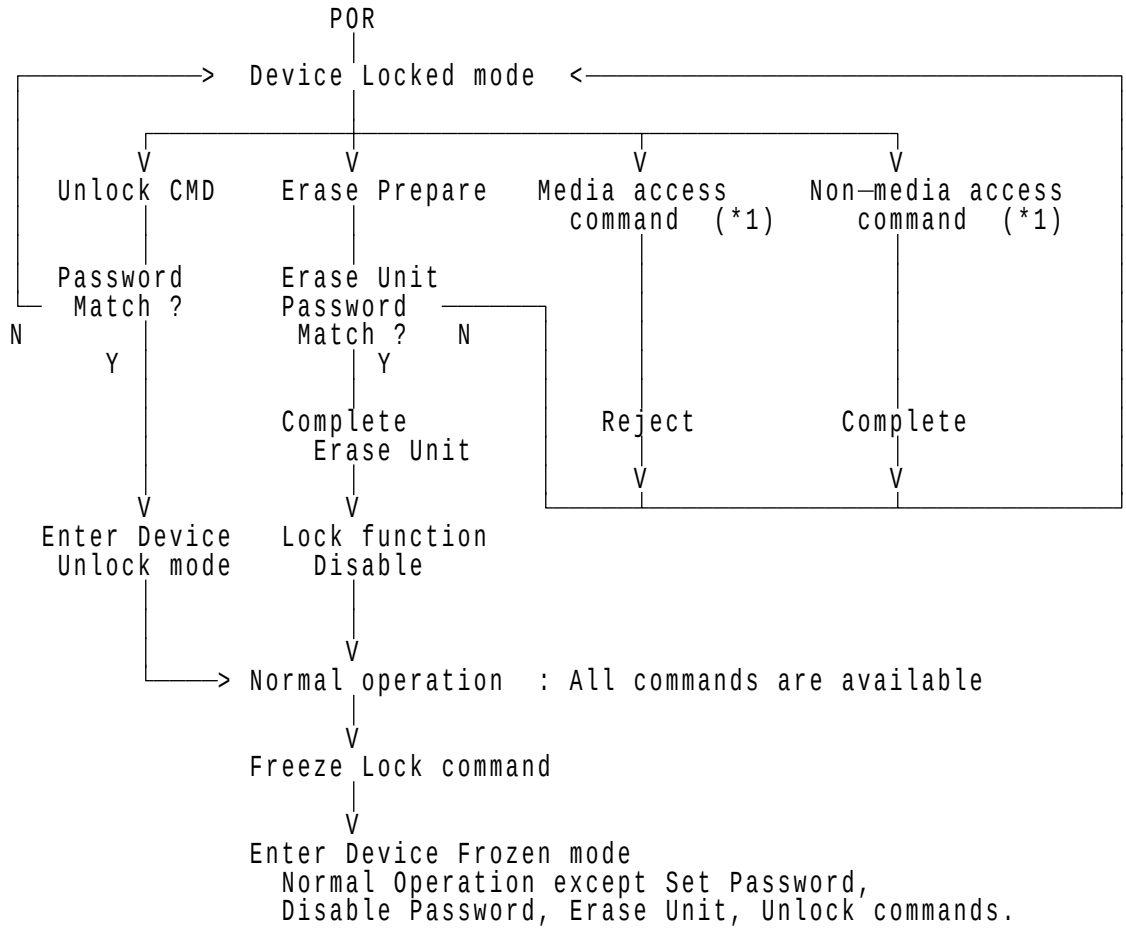


Figure 80. Initial Setting

10.7.4.3 Operation from POR after User Password is set

When Device Lock Function is enabled, the device rejects media access command until a Security Unlock command is successfully completed.



(*1) refer to Figure 83 on page 93

Figure 81. Usual Operation

10.7.4.4 User Password Lost

If the User Password is forgotten and High level security is set, the system user can't access any data. However the device can be unlocked using the Master Password.

If a system user forgets the User Password and Maximum security level is set, data access is impossible. However the device can be unlocked using the Security Erase Unit command to unlock the device and erase all user data with the Master Password.

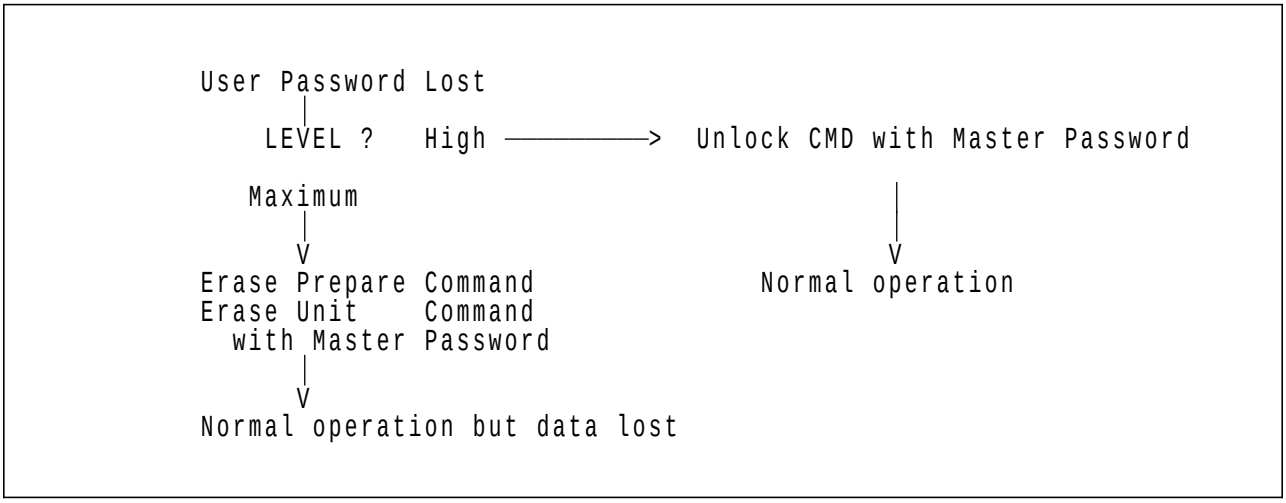


Figure 82. Password Lost

10.7.4.5 Attempt limit for SECURITY UNLOCK command

The SECURITY UNLOCK command has an attempt limit. The purpose of this attempt limit is to prevent that someone attempts to unlock the drive by using various passwords many times.

The device counts the password mismatch. If the password does not match, the device counts it up without distinguishing the Master password and the User password. If the count reaches 5, EXPIRE bit(bit 4) of Word 128 in Identify Device information is set, and then SECURITY ERASE UNIT command and SECURITY UNLOCK command are aborted until a hard reset or a power off. The count and EXPIRE bit are cleared after a power on reset or a hard reset.

10.7.5 Command Table

This table shows the device's response to commands when the Security Mode Feature Set (Device lock function) is enabled.

Command	Locked Mode	Unlocked Mode	Frozen Mode
Check Power Mode	Executable	Executable	Executable
Execute Device Diagnostic	Executable	Executable	Executable
Flush Cache	Executable	Executable	Executable
Format Track	Command aborted	Executable	Executable
Identify Device	Executable	Executable	Executable
Idle	Executable	Executable	Executable
Idle Immediate	Executable	Executable	Executable
Initialize Device Parameters	Executable	Executable	Executable
NOP	Executable	Executable	Executable
Read Buffer	Executable	Executable	Executable
Read DMA (w/o retry)	Command aborted	Executable	Executable
Read DMA (w/retry)	Command aborted	Executable	Executable
Read DMA Queued	Command aborted	Executable	Executable
Read Long (w/o retry)	Command aborted	Executable	Executable
Read Long (w/retry)	Command aborted	Executable	Executable
Read Multiple	Command aborted	Executable	Executable
Read Native Max LBA/CYL	Executable	Executable	Executable
Read Sector(s) (w/o retry)	Command aborted	Executable	Executable
Read Sector(s) (w/retry)	Command aborted	Executable	Executable
Read Verify Sector(s) (w/o retry)	Command aborted	Executable	Executable
Read Verify Sector(s) (w/retry)	Command aborted	Executable	Executable
Recalibrate	Executable	Executable	Executable
Security Disable Password	Command aborted	Executable	Command aborted
Security Erase Prepare	Executable	Executable	Executable
Security Erase Unit	Executable	Executable	Command aborted
Security Freeze Lock	Command aborted	Executable	Executable
Security Set Password	Command aborted	Executable	Command aborted
Security Unlock	Executable	Executable	Command aborted
Seek	Executable	Executable	Executable
Service	Command aborted	Executable	Executable
Set Features	Executable	Executable	Executable
Set Max LBA/CYL	Executable	Executable	Executable
Set Multiple Mode	Executable	Executable	Executable
Sleep	Executable	Executable	Executable
SMART Disable Operations	Executable	Executable	Executable
SMART Enable/Disable Attribute Autosave	Executable	Executable	Executable
SMART Enable Operations	Executable	Executable	Executable
SMART Execute Off-line Immediate	Executable	Executable	Executable
SMART Read Attribute Values	Executable	Executable	Executable
SMART Read Attribute Thresholds	Executable	Executable	Executable
SMART Return Status	Executable	Executable	Executable

Command	Locked Mode	Unlocked Mode	Frozen Mode
SMART Save Attribute Values	Executable	Executable	Executable
SMART Enable/Disable Automatic Off-line Data Collection	Executable	Executable	Executable
Standby	Executable	Executable	Executable
Standby Immediate	Executable	Executable	Executable
Write Buffer	Executable	Executable	Executable
Write DMA (w/o retry)	Command aborted	Executable	Executable
Write DMA (w/retry)	Command aborted	Executable	Executable
Write DMA Queued	Command aborted	Executable	Executable
Write Long (w/o retry)	Command aborted	Executable	Executable
Write Long (w/retry)	Command aborted	Executable	Executable
Write Multiple	Command aborted	Executable	Executable
Write Sector(s) (w/o retry)	Command aborted	Executable	Executable
Write Sector(s) (w/retry)	Command aborted	Executable	Executable
Write Verify	Command aborted	Executable	Executable

Figure 83. Command table for device lock operation

10.8 Protected Area Function

Protected Area Function is to provide the 'protected area' which can not be accessed via conventional method. This 'protected area' is used to contain critical system data such as BIOS or system management information. The contents of entire system main memory may also be dumped into 'protected area' to resume after system power off.

The LBA/CYL changed by following command affects the Identify Device Information.

The following set of commands are implemented for this function.

Read Native Max LBA/CYL ('F8'h)

Set Max LBA/CYL ('F9'h)

10.8.1 Example for operation (In LBA mode)

Assumptions :

For better understanding, following example uses actual values for LBA, size, etc. Since it is just an example, those value could be different.

```
Device characteristics

   Capacity    (native)              : &Capa6.
   Maximum LBA (native)              :    &MaxLBA6.
Required size for protected area     :   &PrtAreaSz6.
Required blocks for protected area   :       &PrtAreaBk6.
Customer usable device size          : &UsrCapa6.
Customer usable sector count         :    &UsrNSec6.
LBA range for protected area         : &PrtLBARng6.
```

1. Shipping HDDs from HDD manufacturer

   When the HDDs are shipped from HDD manufacturer,the device has been tested to have usable capacity of &GBCapa6. besides flagged media defects not to be visible by system.

2. Preparing HDDs at system manufacturer

   Special utility software is required to define the size of protected area and store the data into it. The sequence is :

   Issue Read Native Max LBA/CYL command to get the real device maximum LBA. Returned value shows that native device maximum LBA is &MaxLBA6. regardless of the current setting.

   Make entire device be accessible including the protected area by setting device maximum LBA as &MaxLBA6. via Set Max LBA/CYL command. The option could be either nonvolatile or volatile.

   Test the sectors for protected area (LBA > = &UsrNSec6.) if required.

   Write information data such as BIOS code within the protected area.

   Change maximum LBA using Set Max LBA/CYL command to &UsrSec6. with nonvolatile option.

   From this point, the protected area cannot be accessed till next Set Max LBA/CYL command is issued. Any BIOSes, device drivers, or application software access the HDD as if that is the &GBUsrCapa6. device because the device acts exactly same as real &GBUsrCapa6. device does.

3. Conventional usage without system software support

   Since the HDD works as &GBUsrCapa6. device, there are no special care to use this device for normal use.

4. Advanced usage using protected area

   The data in protected area is accessed by following.

   Issue Read Native Max LBA/CYL command to get the real device maximum LBA. Returned value shows that native device maximum LBA is &MaxLBA6. regardless of the current setting.

   Make entire device be accessible including the protected area by setting device maximum LBA as &MaxLBA6. via Set Max LBA/CYL command with volatile option. By using this option, unexpected power removal or reset will not make the protected area remained accessible.

   Read information data from protected area.

   Issue hard reset or POR to inhibit any access to the protected area.

10.9 Write Cache Function

Write cache is a performance enhancement whereby the device reports as completing the write command (Write Sectors, Write Multiple and Write DMA) to the host as soon as the device has received all of the data into its buffer. And the device assumes responsibility to write the data subsequently onto the disk.

- While writing data after completed acknowledgment of a write command, soft reset or hard reset does not affect its operation. But power off terminates writing operation immediately and unwritten data are to be lost.
- Soft reset, Check Power Mode and Flush Cache commands during writing the cached data are executed after the completion of writing to media. So the host system can confirm the completion of write cache operation by issuing Soft reset, Check Power Mode command or Flush Cache command and then confirming its completion. We developer of the device recommend that a host system checks the completion of write cache operation by issuing Soft reset, Check Power Mode command or Flush Cache command to the device before power off.
- The retry bit of Write Sectors is ignored when write cache is enabled.

10.10 Address Offset Feature (Vendor Specific)

Computer systems perform initial code loading (booting) by reading from a predefined address on a disk drive. To allow an alternate bootable operating system to exist in a reserved area on a disk drive this feature provides a Set Features function to temporarily offset the drive address space. The offset address space wraps around so that the entire disk drive address space remains addressable in offset mode. The Set Max pointer is set to the end of the reserved area to protect the data in the user area when operating in offset mode. This protection can be removed by an Set Max Address command to move the Set Max pointer to the end of the drive. But any commands which access sectors across the original native maximum LBA are rejected with error, even if this protection is removed by an Set Max Address command.

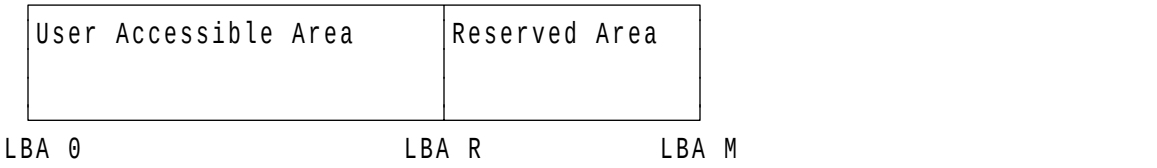
10.10.1 Enable/Disable Address Offset Mode

Subcommand code 09h Enable Address Offset Mode offsets address Cylinder 0, Head 0, Sector 1, LBA 0, to the start of the non-volatile protected area established using the Set Max Address command. The offset condition is cleared by Subcommand 89h Disable Address Offset Mode, Hardware reset or Power on Reset. If Reverting to Power on Defaults has been enabled by Set Features command, it is cleared by Soft reset as well. Upon entering offset mode the capacity of the drive returned in the Identify Device data is the size of the former protected area. A subsequent Set Max Address command with the address returned by Read Max Address command allows access to the entire drive. Addresses wrap so the entire drive remains addressable.

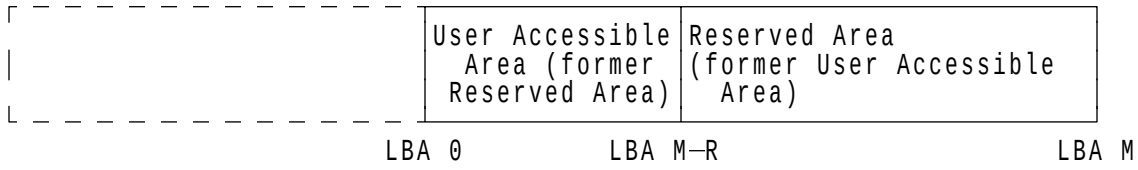
If a non-volatile protected area has not been established before the device receives a Set Features Enable Address Offset Mode command the command fails with Abort error status.

Disable Address Offset Feature removes the address offset and sets the size of the drive reported by the Identify Device command back to the size specified in the last non-volatile Set Max Address command.

– Before Enable Address Offset Mode
A reserved area has been created using a non–volatile Set Max command.



– After Enable Address Offset Mode
The former reserved area is now the user accessible area.
The former user accessible area is now the reserved area.



– After Set Max Address Command using the Value Returned by Read Max Address

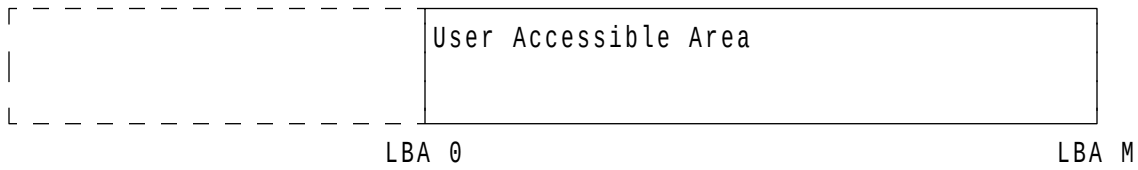


Figure 84. Device address map before and after Set Feature

10.10.2 Identify Device Data

Identify Device data word 83 bit 7 indicates the device supports the Address Offset Feature.

Identify Device data word 86 bit 7 indicates the device is in Address Offset mode.

10.10.3 Exceptions in Address Offset Mode

Any commands which access sectors across the original native maximum LBA are rejected with error, even if the access protection is removed by an Set Max Address command.

Read Look Ahead operation does not be carried out, even if it is enabled by Set Feature command.

10.11 Reassign Function

Reassign Function is used with read commands and write commands. The sectors of data for reassignment are prepared as the spare data sector.

This reassignment information is registered internally, and the information is available right after completing the reassign function. Also the information is used on next power on reset or hard reset.

If the number of the spare sector reaches 0 sector, the reassign function will be disabled automatically.

The spare sectors for reassignment are located at the end of device. As a result of reassignment, the physical location of logically sequenced sectors will be dispersed.

10.11.1 Auto Reassign Function

The sectors those show some errors may be reallocated automatically when specific conditions are met. The spare sectors for reallocation are located at the end of drive. The conditions for auto-reallocation are described below.

Non recovered write errors

When a write operation can not be completed after the Error Recovery Procedure(ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation is failed.

If the write cache function is ENABLED, and when the number of available spare sectors reaches 0 sector, both auto reassign function and write cache function are disabled automatically.

Non recovered read errors

When a read operation is failed after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for the reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

Recovered read errors

When a read operation for a sector failed once then recovered at the specific ERP step, this sector of data is reallocated automatically.

10.12 Automatic Drive Maintenance (ADM)

ADM function is equipped to maintain the reliability even in continuous usage. ADM function is to go into Standby mode automatically after detecting idle mode at intervals of 6 days. This function is always enabled regardless of Standby Timer value.
The detail of Standby Timer is described in 12.6, “Idle (E3h/97h)” on page 122, and 12.32, “Standby (E2h/96h)” on page 171.

The 6 days counter is reset at the following.

- Power on Ready
- Entering Standby mode by Standby Command
- Entering Standby mode by Standby Timer

Both Soft Reset and Hard Reset do not disturb the spin down of ADM.

If a command is received during spin down of ADM, the drive quits the spin down and tries to complete the command as soon as possible.
In case the spin down of ADM is disturbed by a command, it is retried 12 hours later.

For timeout concern, refer to 13.0, “Timeout Values” on page 185.

11.0 Command Protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check if BSY=1, and should proceed no further unless and until BSY=0. For all commands, the host must also wait for RDY=1 before proceeding.

A device must maintain either BSY=1 or DRQ=1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY=1 or DRQ=1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

Figure 142 on page 185 shows the device timeout values.

11.1 PIO Data In Commands

These commands are:

- Identify Device
- Read Buffer
- Read Long
- Read Multiple
- Read Sectors
- SMART Read Attribute Values
- SMART Read Attribute Thresholds

Execution includes the transfer of one or more 512 byte (>512 bytes on Read Long) sectors of data from the device to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
   a. The device sets BSY=1 and prepares for data transfer.
   b. When a sector (or block) of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
   c. In response to the interrupt, the host reads the Status Register.
   d. The device clears the interrupt in response to the Status Register being read.
   e. The host reads one sector (or block) of data via the Data Register.

f. The device sets DRQ=0 after the sector (or block)has been transferred to the host.

4. For the Read Long command:
   a. The device sets BSY=1 and prepares for data transfer.
   b. When the sector of data is available for transfer to the host, the device sets BSY=0, sets DRQ=1, and interrupts the host.
   c. In response to the interrupt, the host reads the Status Register.
   d. The device clears the interrupt in response to the Status Register being read.
   e. The host reads the sector of data including ECC bytes via the Data Register.
   f. The device sets DRQ=0 after the sector has been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register **before** the sector is transferred to the host.

If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an error occurs, the device will set BSY=0, ERR=1, and DRQ=1. The device will then store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The errored location will be reported with CHS mode or LBA mode, the mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

If an Uncorrectable Data Error (UNC=1) occurs, the defective data will be transferred from the media to the sector buffer, and will be available to be transferred to the host, at the host's option. In case of Read Multiple command, the host should complete transfer the block which includes error from the sector buffer and terminate whatever kind of type of error occurred.

If an error occurs that is correctable by retries, the data will be corrected and the transfer will continue normally. There will be no indication to the host that any retry occurred.

All data transfers to the host through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

11.2 PIO Data Out Commands

These commands are:

- Format Track
- Security Disable Password
- Security Erase Unit
- Security Set Password
- Security Unlock
- Write Buffer
- Write Long
- Write Multiple

- Write Sectors

Execution includes the transfer of one or more 512 byte (>512 bytes on Write Long) sectors of data from the host to the device.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. For each sector (or block) of data to be transferred:
   a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector (or block).
   b. The host writes one sector (or block) of data via the Data Register.
   c. The device sets BSY=1 after it has received the sector (or block).
   d. When the device has finished processing the sector (or block), it sets BSY=0, and interrupts the host.
   e. In response to the interrupt, the host reads the Status Register.
   f. The device clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
   a. The device sets BSY=0 and DRQ=1 when it is ready to receive a sector.
   b. The host writes one sector of data including ECC bytes via the Data Register.
   c. The device sets BSY=1 after it has received the sector.
   d. After processing the sector of data the device sets BSY=0 and interrupts the host.
   e. In response to the interrupt, the host reads the Status Register.
   f. The device clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the device detects an invalid parameter, then it will abort the command by setting BSY=0, ERR=1, ABT=1, and interrupting the host.

If an uncorrectable error occurs, the device will set BSY=0 and ERR=1, store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The errored location will be reported with CHS mode or LBA mode, the mode is decided by mode select bit (bit 6) of Device/Head register on issuing the command.

All data transfers to the device through the Data Register are 16 bits, except for the ECC bytes, which are 8 bits.

11.3 Non-Data Commands

These commands are:

- Check Power Mode
- Execute Device Diagnostic
- Flush Cache

- Idle
- Idle Immediate
- Initialize Device Parameters
- NOP
- Read Native Max LBA/CYL
- Read Verify Sectors
- Recalibrate
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Set Features
- Set Max LBA/CYL
- Set Multiple Mode
- Sleep
- SMART Disable Operations
- SMART Enable/Disable Attribute Autosave
- SMART Enable Operations
- SMART Execute Off-line Data Collection
- SMART Return Status
- SMART Save Attribute Values
- SMART Enable/Disable Automatic Off-line Data Collection
- Standby
- Standby Immediate

Execution of these commands involves no data transfer.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY=1.
4. When the device has finished processing the command, it sets BSY=0, and interrupts the host.
5. In response to the interrupt, the host reads the Status Register.
6. The device clears the interrupt in response to the Status Register being read.

11.4 DMA Commands

These commands are:

- Read DMA
- Write DMA

Data transfer using DMA commands differ in two ways from PIO transfers:

- data transfers are performed using the slave-DMA channel
- no intermediate sector interrupts are issued on multi-sector commands

Initiation of the DMA transfer commands is identical to the Read Sector or Write Sector commands except that the host initializes the slave-DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that:

- no intermediate sector interrupts are issued on multi-sector commands
- the host resets the DMA channel prior to reading status from the device.

The DMA protocol allows high performance multi-tasking operating systems to eliminate processor overhead associated with PIO transfers.

1. Host initializes the slave-DMA channel
2. Host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Device/Head registers.
3. Host writes command code to the Command Register
4. The device sets DMARQ when it is ready to transfer any part of the data.
5. Host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the device generates an interrupt to the host.
7. Host resets the slave-DMA channel
8. Host reads the Status Register and, optionally, the Error Register

11.5 DMA Queued Commands

These commands are:

- Read DMA Queued
- Service
- Write DMA Queued

1. Command Issue
   a. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder and Device/Head registers.
   b. The host writes command code to the Command Register
   c. The device sets BSY.
   d. The device clears or sets REL.
   e. The device clears BSY.
2. Data Transfer and Command Completion

   If the device is ready for data transfer (REL is cleared),

   a. The host transfers the data for the command identified by the Tag number using the DMA transfer protocol currently in effect.

b. When all of the data has been transferred, the device generates an interrupt to the host.

c. The host may issue another command or wait for service request from the device.

3. Bus Release

If the device is not ready for data transfer (REL is set),

a. The device generates an interrupt if release interrupt is enabled.

b. The host may issue another command or wait for service request from the device.

12.0 Command Descriptions

Protocol	Command	Code (Hex)	Binary Code Bit 7 6 5 4 3 2 1 0
3	Check Power Mode	E5	1 1 1 0 0 1 0 1
3	Check Power Mode*	98	1 0 0 1 1 0 0 0
3	Execute Device Diagnostic	90	1 0 0 1 0 0 0 0
3	Flush Cache	E7	1 1 1 0 0 1 1 1
2	Format Track	50	0 1 0 1 0 0 0 0
1	Identify Device	EC	1 1 1 0 1 1 0 0
3	Idle	E3	1 1 1 0 0 0 1 1
3	Idle*	97	1 0 0 1 0 1 1 1
3	Idle Immediate	E1	1 1 1 0 0 0 0 1
3	Idle Immediate*	95	1 0 0 1 0 1 0 1
3	Initialize Device Parameters	91	1 0 0 1 0 0 0 1
3	NOP	00	0 0 0 0 0 0 0 0
1	Read Buffer	E4	1 1 1 0 0 1 0 0
4	Read DMA (retry)	C8	1 1 0 0 1 0 0 0
4	Read DMA (no retry)	C9	1 1 0 0 1 0 0 1
5	Read DMA Queued	C7	1 1 0 0 0 1 1 1
1	Read Long (retry)	22	0 0 1 0 0 0 1 0
1	Read Long (no retry)	23	0 0 1 0 0 0 1 1
1	Read Multiple	C4	1 1 0 0 0 1 0 0
3	Read Native Max LBA/CYL	F8	1 1 1 1 1 0 0 0
1	Read Sectors (retry)	20	0 0 1 0 0 0 0 0
1	Read Sectors (no retry)	21	0 0 1 0 0 0 0 1
3	Read Verify Sectors (retry)	40	0 1 0 0 0 0 0 0
3	Read Verify Sectors (no retry)	41	0 1 0 0 0 0 0 1
3	Recalibrate	1x	0 0 0 1 — — — —
2	Security Disable Password	F6	1 1 1 1 1 0 1 0
3	Security Erase Prepare	F3	1 1 1 1 0 0 1 1
2	Security Erase Unit	F4	1 1 1 1 0 1 0 0
3	Security Freeze Lock	F5	1 1 1 1 0 1 0 1
2	Security Set Password	F1	1 1 1 1 0 0 0 1
2	Security Unlock	F2	1 1 1 1 0 0 1 0
3	Seek	7x	0 1 1 1 — — — —
5	Service	A2	1 0 1 0 0 0 1 0
3	Set Features	EF	1 1 1 0 1 1 1 1
3	Set Max LBA/CYL	F9	1 1 1 1 1 0 0 1
3	Set Multiple Mode	C6	1 1 0 0 0 1 1 0

Figure 85. Command Set --- continued ---

Protocol	Command	Code (Hex)	Binary Code Bit 7 6 5 4 3 2 1 0
3	Sleep	E6	1 1 1 0 0 1 1 0
3	Sleep*	99	1 0 0 1 1 0 0 1
3	SMART Disable Operations	B0	1 0 1 1 0 0 0 0
3	SMART Enable/Disable Attribute Autosave	B0	1 0 1 1 0 0 0 0
3	SMART Enable Operations	B0	1 0 1 1 0 0 0 0
3	SMART Execute Off-line Data Collection	B0	1 0 1 1 0 0 0 0
1	SMART Read Attribute Values	B0	1 0 1 1 0 0 0 0
1	SMART Read Attribute Thresholds	B0	1 0 1 1 0 0 0 0
3	SMART Return Status	B0	1 0 1 1 0 0 0 0
3	SMART Save Attribute Values	B0	1 0 1 1 0 0 0 0
3	SMART Enable/Disable Automatic Off-line Data Collection	B0	1 0 1 1 0 0 0 0
3	Standby	E2	1 1 1 0 0 0 1 0
3	Standby*	96	1 0 0 1 0 1 1 0
3	Standby Immediate	E0	1 1 1 0 0 0 0 0
3	Standby Immediate*	94	1 0 0 1 0 1 0 0
2	Write Buffer	E8	1 1 1 0 1 0 0 0
4	Write DMA (retry)	CA	1 1 0 0 1 0 1 0
4	Write DMA (no retry)	CB	1 1 0 0 1 0 1 1
5	Write DMA Queued	CC	1 1 0 0 1 1 0 0
2	Write Long (retry)	32	0 0 1 1 0 0 1 0
2	Write Long (no retry)	33	0 0 1 1 0 0 1 1
2	Write Multiple	C5	1 1 0 0 0 1 0 1
2	Write Sectors (retry)	30	0 0 1 1 0 0 0 0
2	Write Sectors (no retry)	31	0 0 1 1 0 0 0 1

Protocol : 1 : PIO data IN command
2 : PIO data OUT command
3 : Non data command
4 : DMA command
5 : DMA queued command
+ : Vendor specific command

Figure 86. Command Set

Commands marked * are alternate command codes for previous defined commands.

Command (Subcommand)	Command Code (Hex)	Feature Register (Hex)
(S.M.A.R.T function)		
SMART Read Attribute Values	B0	D0
SMART Read Attribute Thresholds	B0	D1
SMART Enable/Disable Attribute Autosave	B0	D2
SMART Save Attribute Values	B0	D3
SMART Execute Off—line Data Collection	B0	D4
SMART Enable Operations	B0	D8
SMART Disable Operations	B0	D9
SMART Return Status	B0	DA
SMART Enable/Disable Automatic Off—line Data Collection	B0	DB
(Set Features)		
Enable Write Cache	EF	02
Set Transfer Mode	EF	03
34 bytes of ECC apply on Read/Write Long	EF	44
Disable read look—ahead feature	EF	55
Enable release interrupt	EF	5D
Disable reverting to power on defaults	EF	66
Disable write cache	EF	82
Enable read look—ahead feature	EF	AA
4 bytes of ECC apply on Read/Wrtie Long	EF	BB
Enable reverting to power on defaults	EF	CC
Disable release interrupt	EF	DD

Figure 87. Command Set (Subcommand)

Figure 85 on page 107 and Figure 86 on page 108 shows the commands that are supported by the device. Figure 87 shows the sub-commands that are supported by each command or feature.

The following symbols are used in the command descriptions:

Output Registers

0	Indicates that the bit must be set to 0.
1	Indicates that the bit must be set to 1.
D	The device number bit. Indicates that the device number bit of the Device/Head Register should be specified. Zero selects the master device and one selects the slave device.
H	Head number. Indicates that the head number part of the Device/Head Register is an output parameter and should be specified.
L	LBA mode. Indicates the addressing mode. Zero specifies CHS mode and one does LBA addressing mode.
R	Retry. Indicates that the Retry bit of the Command Register should be specified.
B	Option Bit. Indicates that the Option Bit of the Sector Count Register should be specified. (This bit is used by Set Max LBA/CYL command)
V	Valid. Indicates that the bit is part of an output parameter and should be specified.
x	Indicates that the hex character is not used.
-	Indicates that the bit is not used.

Input Registers

0	Indicates that the bit is always set to 0.
1	Indicates that the bit is always set to 1.
H	Head number. Indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.
V	Valid. Indicates that the bit is part of an input parameter and will be set to 0 or 1 by the device.
-	Indicates that the bit is not part of an input parameter.

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

12.1 Check Power Mode (E5h/98h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 0 1 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 88. Check Power Mode Command (E5h/98h)

The Check Power Mode command will report whether the device is spun up and the media is available for immediate access.

Input Parameters From The Device

Sector Count The power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the drive is not in Standby or Sleep mode. Otherwise, the Sector Count Register will be set to 0.

12.2 Execute Device Diagnostic (90h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 – – – – –
Command	1 0 0 1 0 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
V	V	V	V	V	V	V	V

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	0

Figure 89. Execute Device Diagnostic Command (90h)

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Figure 77 on page 82 for the definition.

12.3 Flush Cache (E7h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 0 1 1 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 90. Flush Cache Command (E7h)

This command causes the device to complete writing data from its cache.

The device returns good status after data in the write cache is written to disk media.

12.4 Format Track (50h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 1 0 1 0 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	V	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	V	V	–	0	–	V

Figure 91. Format Track Command (50h)

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with write operation. At this time, the sector of data is not verified with read operation whether the sector of data is initialized correctly. Any data previously stored on the track will be lost.

The host may transfer a sector of data containing a format table to the device. But the device ignores the format table and writes zero to all sectors on the track regardless of the descriptors.

Since device performance is optimal at 1:1 interleave, and the device uses relative block addressing internally, the device will always format a track in the same way no matter what sector numbering is specified in the format table.

Output Parameters To The Device

Sector Number In LBA mode, this register specifies LBA address bits 0-7 to be formatted. (L=1)

Cylinder High/Low The cylinder number of the track to be formatted. (L=0)

In LBA mode, this register specifies LBA address bits 8-15 (Low), 16-23 (High) to be formatted. (L=1)

H The head number of the track to be formatted. (L=0)

In LBA mode, this register specifies LBA address bits 24-27 to be formatted. (L=1)

Input Parameters From The Device

Sector Number	In LBA mode, this register specifies current LBA address bits 0-7. (L=1)
Cylinder High/Low	In LBA mode, this register specifies current LBA address bits 8-15 (Low), 16-23 (High)
H	In LBA mode, this register specifies current LBA address bits 24-27. (L=1)
Error	The Error Register. An Abort error (ABT=1) will be returned under the following condition: • No spare data sector to be assigned.

In LBA mode, this command formats a single logical track including the specified LBA.

12.5 Identify Device (ECh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 1 1 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 92. Identify Device Command (ECh)

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information described in Figure 93 on page 117.

Word	Content		Description
00	045AH		Drive classification, bit assignments: 15(=0): 1=ATAPI device, 0=ATA device
		*	14(=0): 1=format speed tolerance gap required
		*	13(=0): 1=track offset option available
		*	12(=0): 1=data strobe offset option available
		*	11(=0): 1=rotational speed tolerance > 0.5%
		*	10(=1): 1=disk transfer rate > 10 Mbps
		*	9(=0): 1=disk transfer rate > 5 Mbps but <= 10 Mbps
		*	8(=0): 1=disk transfer rate <= 5 Mbps
			7(=0): 1=removable cartridge drive
			6(=1): 1=fixed drive
		*	5(=0): 1=spindle motor control option implemented
		*	4(=1): 1=head switch time > 15 us
		*	3(=1): 1=not MFM encoded
		*	2(=0): 1=soft sectored
		*	1(=1): 1=hard sectored
			0(=0): Reserved
01	xxxxH		Number of cylinders in default translate mode
02	0	*	Number of removable cylinders
03	00xxH		Number of heads in default translate mode
04	0	*	Reserved
05	0	*	Reserved
06	003FH		Number of sectors per track in default translate mode
07	0000H	*	Number of bytes of sector gap
08	0000H	*	Number of bytes in sync field
09	0000H	*	Reserved
10–19	XXXX		Serial number in ASCII (0 = not specified)
20	0003H	*	Controller type: 0003: dual ported, multiple sector buffer with look–ahead read
21	XXXXH	*	Buffer size in 512–byte increments A value between 03A0H and 03B1H (model dependent)
22	0022H	*	Number of ECC bytes (Vendor unique length selected via set feature cmd)
23–26	XXXX		Microcode version in ASCII
27–46	XXXX		Model number in ASCII
47	8010H		15–8 80h 7–0 Maximum number of sectors that can be transferred per interrupt on Read and Write Multiple commands
48	0000H		Reserved

Figure 93. Identify device information

Word	Content	Description
49	xF00H	Capabilities, bit assignments: 15–14(=0) Reserved 13 Standby timer (=1) values as specified in ATA standard are supported (=0) values are vendor specific 12(=0) Reserved 11(=1) IORDY Supported 10(=1) IORDY can be disabled 9(=1) Reserved 8(=1) Reserved
	*	7– 0(=0) Reserved
50	400xH	Capabilities, bit assignments: 15–14(=01) Word 50 is valid 13– 1(=0) Reserved 0 Minimum value of Standby timer (=0) less than 5 minutes (=1) equal to or greater than 5 minutes
51	0200H	PIO data transfer cycle timing mode
52	0200H *	DMA data transfer cycle timing mode Refer Word 62 and 63
53	0007H	Validity flag of the word 15– 3(=0) Reserved 2(=1) 1=Word 88 are Valid 1(=1) 1=Word 64–70 are Valid 0(=1) 1=Word 54–58 are Valid
54	xxxxH	Number of current cylinders
55	xxxxH	Number of current heads
56	xxxxH	Number of current sectors per track
57–58	xxxxH	Current capacity in sectors Word 57 specifies the low word of the capacity
59	0xxxH	Current Multiple setting. bit assignments 15– 9(=0) Reserved 8 1= Multiple Sector Setting is Valid 7– 0 xxh = Current setting for number of sectors
60–61	xxxxH	Total Number of User Addressable Sectors Word 60 specifies the low word of the number
62	0000H *	Single Word DMA Transfer Capability 15– 8 Single word DMA transfer mode active 7– 0(=7) Single word DMA transfer modes supported (not supported)
63	xx07H	Multiword DMA Transfer Capability 15– 8 Multi word DMA transfer mode active 7– 0(=7) Multi word DMA transfer modes supported (support mode 0,1 and 2)
64	0003H	Flow Control PIO Transfer Modes Supported 15– 8(=0) Reserved 7– 0(=3) Advanced PIO Transfer Modes Supported '11' = PIO Mode 3 and 4 Supported
65	0078H	Minimum Multiword DMA Transfer Cycle Time Per Word 15– 0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)

Figure 94. Identify device information --- Continued ---

Word	Content	Description
66	0078H	Manufacturer's Recommended Multiword DMA Transfer Cycle Time 15– 0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
67	00F0H	Minimum PIO Transfer Cycle Time Without Flow Control 15– 0(=F0) Cycle time in nanoseconds (240ns, 8.3MB/s)
68	0078H	Minimum PIO Transfer Cycle Time With IORDY Flow Control 15– 0(=78) Cycle time in nanoseconds (120ns, 16.6MB/s)
69–74	0000H	Reserved
75	00xxH	Queue depth 15– 5 Reserved 4– 0 Maximum queue depth
76–79	0000H	Reserved
80	001EH	Major version number 15– 0(=1E) ATA–1, ATA–2, ATA–3 and ATA/ATAPI–4
81	0017H	Minor version number 15– 0(=11) ATA/ATAPI–4 X3T13 1153D revision 17
82	74EBH	Command set supported 15(=0) Reserved 14(=1) NOP command 13(=1) READ BUFFER command 12(=1) WRITE BUFFER command 11(=0) Reserved 10(=1) Host Protected Area feature set 9(=0) DEVICE RESET command 8(=0) SERVICE interrupt 7(=1) RELEASE interrupt 6(=1) LOOK AHEAD 5(=1) WRITE CACHE 4(=0) PACKET Command feature set 3(=1) Power management feature set 2(=0) Removable feature set 1(=1) Security feature set 0(=1) SMART feature set
83	4082H	Command set supported 15–14(=01) Word 83 is valid 13– 8(=0) Reserved 7(=1) Set Features Address Offset mode 6(=0) Reserved 5(=0) Reserved 4(=0) Removable Media Status Notification feature 3(=0) Advanced Power management feature set 2(=0) CFA feature set 1(=1) READ/WRITE DMA QUEUED 0(=0) DOWNLOAD MICROCODE command
84	4000H	Command set/feature supported extension 15–14(=01) Word 84 is valid 13– 0(=0) Reserved

Figure 95. Identify device information --- Continued ---

Word	Content	Description
85	xxxxH	Command set/feature enebled 15 Reserved 14 NOP command 13 READ BUFFER command 12 WRITE BUFFER command 11 Reserved 10 Host Protected Area feature set 9 DEVICE RESET command 8 SERVICE interrupt 7 RELEASE interrupt 6 LOOK AHEAD 5 WRITE CACHE 4 PACKET Command feature set 3 Power management feature set 2 Removable feature set 1 Security feature set 0 SMART feature set
86	xxxxH	Command set/feature enebled 15– 8 Reserved 7 Set Features Address Offset mode 6 Reserved 5 Reserved 4 Removable Media Status Notification feature 3 Advanced Power management feature set 2 CFA feature set 1 READ/WRITE DMA QUEUED 0 DOWNLOAD MICROCODE command
87	4000H	Command set/feature default 15–14(=01) Word 87 is valid 13– 0(=0) Reserved
88	0x1FH	Ultra DMA transfer modes 15– 8(=xx) Current active Ultra DMA transfer mode 15–13 Reserved (=0) 12 Mode 4 1= Active 0= Not Active 11 Mode 3 1= Active 0= Not Active 10 Mode 2 1= Active 0= Not Active 9 Mode 1 1= Active 0= Not Active 8 Mode 0 1= Active 0= Not Active 7– 0(=1F) Ultra DMA transfer mode supported 7– 5 Reserved (=0) 4 Mode 4 1= Support 3 Mode 3 1= Support 2 Mode 2 1= Support 1 Mode 1 1= Support 0 Mode 0 1= Support

Figure 96. Identify device information --- Continued ---

Word	Content	Description
89	xxxxH	Time required for security erase unit complition Time = value * 2 (minutes)
90	0000H	Time required for Enhanced security erase complition
91	0000H	Current advanced power management value
92–126	0000H	Reserved
127	0000H	Removable Media Status Notification feature set 0000H = Not supported
128	xxxxH	Device Lock Function. Bit assignments 15– 9 Reserved 8 Security Level 1= Maximum, 0= High 7– 6 reserved 5 Enhanced erase 1= Support 4 Expire 1= Expired 3 Freeze 1= Frozen 2 Lock 1= Locked 1 Enable/Disable 1= Enable 0 Capability 1= Support
129	xxxxH *	Current Set Feature Option. Bit assignments 15– 4 Reserved 3 Auto reassign 1= Enable 2 Reverting 1= Enable 1 Read Look–ahead 1= Enable 0 Write Cache 1= Enable
130–159	xxxxH *	Reserved
160–255	0000H	Reserved

Figure 97. Identify device information --- Continued ---

Note. The '*' mark in 'Content' field indicates the use of those parameters are vendor specific.

12.6 Idle (E3h/97h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 0 0 1 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 98. Idle Command (E3h/97h)

The Idle command causes the device to enter Idle mode immediately, and set auto power down timeout parameter(standby timer). And then the timer starts counting down.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

Output Parameters To The Device

Sector Count Timeout Parameter. If zero, then the automatic power down sequence is disabled. If non-zero,then the automatic power down sequence is enabled,and the timeout interval is shown blow:

Value	Timeout
0	Timer disabled
1 - 240	Value * 5 seconds
241 - 251	(Value-240) * 30 minutes
252	21 minutes
253	8 hours
254	21 minutes 10 seconds
255	21 minutes 15 seconds

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

12.7 Idle Immediate (E1h/95h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 0 0 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 99. Idle Immediate Command (E1h/95h)

The Idle Immediate command causes the device to enter Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to host commands immediately.

The Idle Immediate command will not affect to auto power down timeout parameter.

12.8 Initialize Device Parameters (91h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D H H H H
Command	1 0 0 1 0 0 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 100. Initialize Device Parameters Command (91h)

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54-58 in Identify Device Information reflects these parameters.

The parameters remain in effect until following events:

- Another Initialize Device Parameters command is received.
- The device is powered off.
- Soft reset/Hard reset is occurred and the Set Feature option of CCh is set instead of 66h.

Output Parameters To The Device

Sector Count The number of sectors per track. 0 does not mean there are 256 sectors per track, but there is no sector per track.

H The number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

Note: The following conditions needs to be satisfied to avoid invalid number of cylinders beyond FFFFh.

(Total number of user addressable sectors)/((Sector Count)*(H+1)) = < FFFFh

The total number of user addressable sectors is described in Identify Device command.

12.9 NOP (00h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	V V V V V V V V
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	0 0 0 0 0 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	Initial value
Sector Number	Initial value
Cylinder Low	Initial value
Cylinder High	Initial value
Device/Head	Initial value
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 101. NOP Command (00h)

This command always fails with an error. The device responds with command aborted.

Output Parameters To The Device

Feature Subcommand code.

00H Abort any outstanding queue.

01H - FFH Not abort any outstanding queue.

The value of Sector Count, Sector Number, Cylinder High/Low, Device/Head set by host is not changed.

12.10 Read Buffer (E4h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 0 1 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 102. Read Buffer Command (E4h)

The Read Buffer command transfers a sector of data from the sector buffer of device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

12.11 Read DMA (C8h/C9h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 1 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
V	0	0	V	0	V	0	V

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 103. Read DMA Command (C8h/C9h)

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register specifies LBA address bits 0 - 7 to be transferred. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register specifies LBA address bits 8 - 15 (Low) 16 - 23 (High) to be transferred. (L=1)

H	The head number of the first sector to be transferred. (L=0)
	In LBA mode, this register specifies LBA bits 24-27 to be transferred. (L=1)
R	The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0)
	In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.12 Read DMA Queued (C7h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	V V V V V V V V
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 0 1 1 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
V	0	0	V	0	V	0	V

Status Register							
7 BSY	6 RDY	5 DF	4 SRV	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 104. Read DMA Queued Command (C7h)

This command executes in a similar manner to a READ DMA command. The device may perform a bus release or it may execute the data transfer without performing a bus release if the data is ready to transfer.

If the device performs a bus release, the host shall reselect the device using the SERVICE command.

Once the data transfer is begun, the device does not perform a bus release until the entire data transfer has been completed.

Output Parameters To The Device

Feature number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Count bits 7 - 3 (Tag) contain the Tag for the command being delivered.

Sector Number starting sector number or LBA address bits 7 - 0.

Cylinder High/Low starting cylinder number or LBA address bits 23 - 8.

H starting head number or LBA address bits 27 - 24.

Input Parameters From The Device On Bus Release

Sector Count bits 7 - 3 (Tag) contain the Tag of the command being bus released.

bit 2 (REL) is set to one.

bit 1 (I/O) is cleared to zero.

bit 0 (C/D) is cleared to zero.

Sector Number, Cylinder High/Low, H n/a.

SRV cleared to zero when the device performs a bus release. This bit is set to one when the device is ready to transfer data.

Input Parameters From The Device On Command Complete

Sector Count bits 7 - 3 (Tag) contain the Tag of the completed command.

bit 2 (REL) is cleared to zero.

bit 1 (I/O) is set to one.

bit 0 (C/D) is set to one.

Sector Number, Cylinder High/Low, H sector address of unrecoverable error. (applicable only when unrecoverable error has occurred.)

SRV cleared to zero.

12.13 Read Long (22h/23h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	0 0 0 0 0 0 0 1
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 0 0 0 1 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – – V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	V	0	V	0	V

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 105. Read Long Command (22h/23h)

The Read Long command read the designated one sector of data and the ECC bytes from disk media, then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 34 according to setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC, whatever is read is returned to the host.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number The sector number of the sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H	The head number of the sector to be transferred. (L=0)
	In LBA mode, this register contains LBA bits 24-27. (L=1)
R	The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 24-27. (L=1)

It should be noted that the device internally uses 34 bytes of ECC data on all data written or read from the disk. The 4 byte mode of operation is provided via an emulation. It is recommended that for testing the effectiveness and integrity of the devices ECC functions that the 34 byte ECC mode should be used.

12.14 Read Multiple (C4h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 0 1 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	V	0	V	0	V	0	V

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 106. Read Multiple Command (C4h)

The Read Multiple command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.15 Read Native Max LBA/CYL (F8h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 L 1 D – – – –
Command	1 1 1 1 1 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 107. Read Native Max LBA/CYL (F8h)

This command returns the native max LBA/CYL of HDD which is not effected by Set Max LBA/CYL command.

Input Parameters From The Device

Sector Number In LBA mode, this register contains native max LBA bits 0 - 7. (L=1)

In CHS mode, this register contains native max sector number. (L=0)

Cylinder High/Low In LBA mode, this register contains native max LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

In CHS mode, this register contains native max cylinder number. (L=0)

H In LBA mode, this register contains native max LBA bits 24 - 27. (L=1)

In CHS mode, this register contains native max head number.(L=0)

12.16 Read Sectors (20h/21h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 0 0 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	V	0	V	0	V	0	V

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 108. Read Sectors Command (20h/21h)

The Read Sectors command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.17 Read Verify Sectors (40h/41h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 0 0 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	V	0	V	0	V	0	V

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 109. Read Verify Sectors Command (40h/41h)

The Read Verify Sectors verifies one or more sectors on the device. No data is transferred to the host.

The difference of Read Sectors command and Read Verify Sectors command is whether the data is transferred to the host or not.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be verified. If zero is specified, then 256 sectors will be verified.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not verified. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.18 Recalibrate (1xh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	0 0 0 1 – – – –

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	V	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 110. Recalibrate Command (1xh)

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0.

If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

12.19 Security Disable Password (F6h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 1 0 1 1 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 111. Security Disable Password Command (F6h)

The Security Disable Password command disables the security mode feature (device lock function).

The Security Disable Password command requests a transfer of a single sector of data from the host including information specified in Figure 112. Then the device checks the transferred password. If the User Password or Master Password matches the given password, the device disables the security mode feature (device lock function). This command does not change the Master Password which may be re-activated later by setting User Password. This command should be executed in device unlock mode.

Word	Description
00	Control word bit 0 : Identifier (1– Master, 0– User) bit 1–15 : Reserved
01–16	Password (32 bytes)
17–255	Reserved

Figure 112. Password Information for Security Disable Password command

The device will compare the password sent from this host with that specified in the control word.

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

12.20 Security Erase Prepare (F3h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 1 0 0 1 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 113. Security Erase Prepare Command (F3h)

The Security Erase Prepare Command must be issued immediately before the Security Erase Unit Command to enable device erasing and unlocking.

The Security Erase Prepare Command must be issued immediately before the Format Unit Command. This command is to prevent accidental erasure of the device.

This command does not request to transfer data.

12.21 Security Erase Unit (F4h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 1 0 1 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	V	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 114. Security Erase Unit Command (F4h)

The Security Erase Unit command initializes all user data sectors, then disables the device lock function.

Note that the Security Erase Unit command initializes from LBA 0 to Native MAX LBA. Host MAX LBA set by Initialize Drive Parameter or Set MAX LBA/CYL command is ignored. So the protected area by Set MAX LBA/CYL command is also initialized.

This command requests to transfer a single sector data from the host including information specified in Figure 115.

If the password does not match then the device rejects the command with an Aborted error.

Word	Description
00	Control word bit 0 : Identifier (1– Master, 0– User) bit 1 : Erase mode (1– Enhanced, 0– Normal) Enhanced mode is not supported bit 2–15 : Reserved
01–16	Password (32 bytes)
17–255	Reserved

Figure 115. Erase Unit information

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

The Security Erase Unit command erases all user data and disables the security mode feature (device lock function). So after completing this command, all user data will be initialized to zero with write operation. At this time, it is not verified with read operation whether the sector of data is initialized correctly. Also, the defective sector information and the reassigned sector information for the device are not updated. The security erase prepare command should be completed immediately prior to the Security Erase Unit command. If the device receives a Security Erase Unit command without a prior Security Erase Prepare command the device aborts the security erase unit command.

This command disables the security mode feature (device lock function), however the master password is still stored internally within the device and may be re-activated later when a new user password is set. If you execute this command on disabling the security mode feature (device lock function), the password sent by the host is NOT compared with the password stored in the device for both the Master Password and the User Password, and then the device only erases all user data.

The execution time of this command is set in word 89 of Identify device information.

12.22 Security Freeze Lock (F5h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 1 0 1 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 116. Security Freeze Lock Command (F5h)

The Security Freeze Lock Command allows the device to enter frozen mode immediately.

After this command is completed, the command which updates Security Mode Feature (Device Lock Function) is rejected.

Frozen mode is quit only by Power off.

The following commands are rejected when the device is in frozen mode. For detail, refer to Figure 83 on page 93.

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

12.23 Security Set Password (F1h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 1 0 0 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 117. Security Set Password Command (F1h)

The Security Set Password command enables security mode feature (device lock function), and sets the master password or the user password.

The security mode feature (device lock function) is enabled by this command, and the device is not locked immediately. The device is locked after next power on reset or hard reset. When the MASTER password is set by this command, the master password is registerred internally, but the device is NOT locked after next power on reset or hard reset.

This command requests a transfer of a single sector of data from the host including the information specified in Figure 118 on page 148.

The data transferred controls the function of this command.

Word	Description
00	Control word bit 0 : Identifier (1– Master, 0– User) bit 1–7 : Reserved bit 8 : Security level (1– Maximum, 0– High) bit 9–15 : Reserved
01–16	Password (32 byte)
17–255	Reserved

Figure 118. Security Set Password Information

Identifier Zero indicates that device regards Password as User Password. One indicates that device regards Password as Master Password.

Security Level Zero indicates High level, one indicates Maximum level. If the host sets High level and the password is forgotten, then the Master Password can be used to unlock the device. If the host sets Maximum level and the user password is forgotten, only an Security Erase Prepare/Security Unit command can unlock the device and all data will be lost.

Password The text of the password - all 32 bytes are always significant.

The setting of the Identifier and Security level bits interact as follows.

Identifier=User / Security level = High The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by either the user password or the previously set master password.

Identifier=Master / Security level = High This combination will set a master password but will NOT enable the security mode feature (lock function).

Identifier=User / Security level = Maximum The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The file may then be unlocked by only the user password. The master password previously set is still stored in the file but may NOT be used to unlock the device.

Identifier=Master / Security level = Maximum This combination will set a master password but will NOT enable the security mode feature (lock function).

12.24 Security Unlock (F2h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 1 0 0 1 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	V	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 119. Security Unlock Command (F2h)

This command unlocks the password and causes the device to enter device unlock mode. If power on reset or hard reset is done without executing the Security Disable Password command after this command is completed, the device will be in device lock mode. The password has not been changed yet.

The Security Unlock command requests to transfer a single sector of data from the host including information specified in Figure 120 on page 150.

If the Identifier bit is set to master and the file is in high security mode then the password supplied will be compared with the stored master password. If the file is in maximum security mode then the security unlock will be rejected.

If the Identifier bit is set to user, then the file compares the supplied password with the stored user password.

If the password compare fails then the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch. When this counter reaches zero then all password protected commands are rejected until a hard reset or a power off.

Word	Description
00	Control word bit 0 : Identifier (1– Master, 0– User) bit 1–15 : Reserved
01–16	Password (32 bytes)
17–255	Reserved

Figure 120. Security Unlock Information

Identifier Zero indicates that device regards Password as User Password. One indicates that device regards Password as Master Password.

The user can detect if the attempt to unlock the device has failed due to a mismatched password as this is the only reason that an abort error will be returned by the file AFTER the password information has been sent to the device. If an abort error is returned by the device BEFORE the password data has been sent to the file then another problem exists.

12.25 Seek (7xh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 1 1 1 – – – –

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	V	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 121. Seek Command (7xh)

The Seek command initiates a seek to the designated track and selects the designated head. The device need not be formatted for a seek to execute properly.

Output Parameters To The Device

Sector Number In LBA mode, this register specifies LBA address bits 0 - 7 for seek. (L=1)

Cylinder High/Low The cylinder number of the seek.

In LBA mode, this register specifies LBA address bits 8 - 15 (Low), 16 - 23 (High) for seek. (L=1)

H The head number of the seek.

In LBA mode, this register specifies LBA address bits 24 - 27 for seek. (L=1)

Input Parameters From The Device

Sector Number In LBA mode, this register contains current LBA bits 0 - 7. (L=1)

Cylinder High/Low In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.26 Service (A2h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – D – – – –
Command	1 0 1 0 0 0 1 0

Figure 122. Service Command (A2h)

The Service command is used to provide data transfer and/or status of a command that was previously bus released.

Output Parameters To The Device

D selected device.

Input Parameters From The Device

Input from the device as a result of a Service command are described in the command description for the command for which Service is being requested.

12.27 Set Features (EFh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	V V V V V V V V
Sector Count	Note.1
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 1 1 1 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 123. Set Features Command (EFh)

The Set Feature command is to establish the following parameters which affect the execution of certain features as shown in below table.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

Output Parameters To The Device

Feature Destination code for this command.

02H Enable write cache

03H Set transfer mode based on value in sector count register

09H Enable Address Offset mode

44H 34 bytes of ECC apply on Read Long/Write Long commands

55H Disable read look-ahead feature

5DH Enable release interrupt

66H Disable reverting to power on defaults

82H Disable write cache

89H Disable Address Offset mode

AAH Enable read look-ahead feature

BBH 4 bytes of ECC apply on Read Long/Write Long commands

CCH Enable reverting to power on defaults

DDH Disable release interrupt

Note 1.

When Feature register is 03h (=Set Transfer mode), the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

```
PIO Default Transfer Mode                00000 000
PIO Default Transfer Mode,Disable IORDY  00000 001
PIO Flow Control Transfer Mode x         00001 nnn (nnn=000,001,010,011,100)
Multiword DMA mode x                     00100 nnn (nnn=000,001,010)
Ultra DMA mode x                         01000 nnn (nnn=000,001,010,011,100)
```

Note 2.

If the number of auto reassigned sector reaches the device's reassignment capacity, the write cache function will be automatically disabled. Although the device still accepts the Set Features command with Feature register = 02h without error, but the write cache function will remains disabled. For current write cache function status, please refer to Identify Device Information(word 85 or 129) by Identify Device command.

Note 3.

After power on reset or hard reset, the device is set to the following features as default.

```
Write cache                     :  Enable
ECC bytes                       :  4 bytes
Read look-ahead                 :  Enable
Reverting to power on defaults  :  Disable
Release interrupt               :  Disable
```

12.28 Set Max LBA/CYL (F9h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – B
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 1 1 1 0 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 124. Set Max LBA/CYL (F9h)

This command overwrites the maximum number of LBA/CYL of HDD in a range of actual device capacity. Once device receives this command, all accesses beyond that LBA/CYL are rejected with setting ABORT bit in status register. Identify device command returns the LBA/CYL which is set via this command as a default value.

Read Native Max LBA/CYL command should be issued and completed immediately prior to issuing Set Max LBA/CYL command. If the device receives Set Max LBA/CYL command without a prior Read Native Max LBA/CYL command, the device aborts the Set Max LBA/CYL.

If the device receives this command that changes maximum number of LBA or Cylinder to 0, the device returns aborted error to the host.

If the device in Address Offset mode receives this command with the nonvolatile option, the device returns aborted error to the host.

Output Parameters To The Device

B Option bit for selection whether nonvolatile or volatile. B=0 is volatile condition. When B=1, MAX LBA/CYL which is set by Set Max LBA/CYL command is preserved by POR. When B=0, MAX LBA/CYL which is set by Set Max LBA/CYL command will be lost by POR. B=1 is not valid when the device is in Address Offset mode.

Sector Number	In LBA mode, this register contains LBA bits 0 - 7 which is to be set.(L=1)
	In CHS mode, this register is ignored. (L=0)
Cylinder High/Low	In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High) which is to be set. (L=1)
	In CHS mode, this register contains cylinder number which is to be set.(L=0)
H	In LBA mode, this register contains LBA bits 24 - 27 which is to be set.(L=1)
	In CHS mode, this register is ignored. (L=0)

Input Parameters From The Device

Sector Number	In LBA mode, this register contains max LBA bits 0 - 7 which is set.(L=1)
	In CHS mode, this register contains max sector number. (L=0)
Cylinder High/Low	In LBA mode, this register contains max LBA bits 8 - 15 (Low), 16 - 23 (High) which is set. (L=1)
	In CHS mode, this register contains max cylinder number which is set. (L=0)
H	In LBA mode, this register contains max LBA bits 24 - 27 which is set. (L=1)
	In CHS mode, this register contains max head number.(L=0)

12.29 Set Multiple (C6h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 0 0 0 1 1 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 125. Set Multiple Command (C6h)

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

If an invalid block size is specified, an Abort error will be returned to the host, and Read Multiple and Write Multiple commands will be disabled.

Output Parameters To The Device

Sector Count. The block size to be used for Read Multiple and Write Multiple commands. Valid block sizes can be selected from 0, 2, 4, 8 or 16. If 0 is specified, then Read Multiple and Write Multiple commands are disabled.

12.30 Sleep (E6h/99h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 0 1 1 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 126. Sleep Command (E6h/99h)

This command causes the device to enter Sleep Mode.

The device is spun down and the interface becomes inactive. If the device is already spun down, the spin down sequence is not executed.

The only way to recover from Sleep Mode is with a software reset or a hardware reset.

12.31 S.M.A.R.T. Function Set (B0h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	V V V V V V V V
Sector Count	V V V V V V V V
Sector Number	– – – – – – – –
Cylinder Low	0 1 0 0 1 1 1 1
Cylinder High	1 1 0 0 0 0 1 0
Device/Head	1 – 1 D – – – –
Command	1 0 1 1 0 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 127. S.M.A.R.T. Function Set Command (B0h)

The S.M.A.R.T. Function Set command provides access to Attribute Values, Attribute Thresholds and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The S.M.A.R.T. Function Set command has several separate subcommands which are selectable via the device's Features Register when the S.M.A.R.T. Function Set command is issued by the host.

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

Code	Subcommand
D0h	SMART Read Attribute Values
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/disable Attribute Autosave
D3h	SMART Save Attribute Values
D4h	SMART Execute Off-line Data Collection
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
DBh	SMART Enable/Disable Automatic Off-Line Data Collection

12.31.1.1 SMART Read Attribute Values (Subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the SMART Read Attribute Values subcommand from the host, the device saves any updated Attribute Values to the Attribute Data sectors, and then transfers the 512 bytes of Attribute Value information to the host.

12.31.1.2 SMART Read Attribute Thresholds (Subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the SMART Read Attribute Thresholds subcommand from the host, the device reads the Attribute Thresholds from the Attribute Threshold sectors, and then transfers the 512 bytes of Attribute Thresholds information to the host.

12.31.1.3 SMART Enable/Disable Attribute Autosave (Subcommand D2h)

This subcommand enables and disables the attribute autosave feature of the device. The SMART Enable/Disable Attribute Autosave subcommand either allows the device to automatically save its updated Attribute Values to the Attribute Data Sector periodically; or this subcommand causes the autosave feature to be disabled. The state of the Attribute Autosave feature (either enabled or disabled) will be preserved by the device across power cycle.

A value of 00h written by the host into the device's Sector Count Register before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or power-down.

A value of F1h written by the host into the device's Sector Count Register before issuing the SMART Enable/Disable Attribute Autosave subcommand will cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing the SMART Enable/Disable Attribute Autosave subcommand will not change the current Autosave status but the device will respond with the error code specified in Figure 133 on page 170.

The SMART Disable Operations subcommand disables the autosave feature along with the device's SMART operations.

Upon the receipt of the subcommand from the host, the device asserts BSY, enables or disables the Autosave feature, clears BSY and asserts INTRQ.

12.31.1.4 SMART Save Attribute Values (Subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the SMART Save Attribute Values subcommand from the host, the device writes any updated Attribute Values to the Attribute Data sector.

12.31.1.5 SMART Execute Off-line Data Collection (Subcommand D4h)

This subcommand causes the device to immediately initiate or resume the set of activities that collect Attribute data in an off-line mode.

If the device is in the process of performing its set of off-line activities as a result of receiving a S.M.A.R.T. Execute Off-line Data Collection subcommand from the host and is interrupted by a new command from the host, the device will suspend its off-line activities and service the host within two seconds after receipt of the new command. The device will resume Off-line data collection activity automatically.

Upon receipt of the subcommand from the host, the device sets BSY to one, begins its set of off-line activities, clears BSY to zero and asserts INTRQ.

During execution of its off-line activities the device will not set BSY nor clear DRDY.

12.31.1.6 SMART Enable Operations (Subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of an SMART Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T. (either enabled or disabled) will be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART Enable Operations subcommands will not affect any of the Attribute Values.

Upon receipt of the SMART Enable Operations subcommand from the host, the device enables S.M.A.R.T. capabilities and functions, and then saves any updated Attribute Values to the Attribute Data sector.

12.31.1.7 SMART Disable Operations (Subcommand D9h)

This subcommand disables all S.M.A.R.T.capabilities within the device including the device's attribute autosave feature. After receipt of this subcommand the device disables all S.M.A.R.T. operations. Non self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T. (either enabled or disabled) is preserved by the device across power cycles.

Upon receipt of the SMART Disable Operations subcommand from the host, the device disables S.M.A.R.T. capabilities and functions, and then saves any updated Attribute Values to the Attribute Data sector.

After receipt of the device of the SMART Disable Operations subcommand from the host, all other S.M.A.R.T. subcommands -- with the exception of SMART Enable Operations -- are disabled and invalid and will be aborted by the device (including the SMART Disable Operations subcommand), returning the error code as specified in Figure 133 on page 170.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the SMART Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a SMART Read Attribute Values or SMART Save Attribute Values command.

12.31.1.8 SMART Return Status (Subcommand DAh)

This command is used to communicate the reliability status of the device to the host's request. Upon receipt of the SMART Return Status subcommand the device saves any updated Pre-failure type Attribute Values to the reserved sector and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, the device loads 4Fh into the Cylinder Low register, C2h into the Cylinder High register.

If the device detect a Threshold Exceeded Condition, the device loads F4h into the Cylinder Low register, 2Ch into the Cylinder High register.

12.31.1.9 SMART Enable/Disable Automatic Off-Line Data Collection (Subcommand DBh)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's non-volatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled.

A value of zero written by the host into the device's Sector Count register before issuing this subcommand shall cause the feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to non-volatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F8h written by the host into the device's Sector Count register before issuing this subcommand shall cause this feature to be enabled. Any other non-zero value written by the host into this register before issuing this subcommand is vender specific and will not change the current Automatic Off-Line Data Collection status, but device may respond with the error code specified in Figure 133 on page 170.

12.31.2 Device Attributes Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Values subcommand. All multi-byte fields shown in these data structures follow the ATA/ATAPI-4 specifications for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

Description	Bytes	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0005h
1st Device Attribute	12	02h	(*1)	(*2)
...	..			
...	..			
30th Device Attribute	12	15Eh	(*1)	(*2)
Off–line data collection status	1	16Ah	(*1)	(*2)
Total segments required for off–line data collection	1	16Bh	(*1)	01h
Total time in seconds to complete next segment	2	16Ch	(*1)	(*2)
Current segment pointer	1	16Eh	(*1)	(*2)
Off–line data collection capability	1	16Fh	(*1)	0Bh
S.M.A.R.T. capability	2	170h	(*1)	03h
Reserved	16	172h		(*3)
Vendor specific	125	182h		(*3)
Data structure checksum	1	1FFh		(*2)
	512			

(*1) – See following definitions
(*2) – Value varied by actual operating condition
(*3) – Filled with 00h

Figure 128. Device Attribute Data Structure

12.31.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number will be set to 0005h. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

12.31.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Description	Bytes	Offset	Format
Attribute ID Number (01h to FFh)	1	00h	binary
Status Flags	2	01h	bit flags
Pre–Failure/Advisory bit			
On–line Collection bit			
Vendor Specific (4 bits)			
Reserved (10 bits, all 0)			
Attribute Value (valid values from 01h to FEh)	1	03h	binary
00h invalid for attribute value – not to be used			
01h minimum value			
64h initial value for all attributes prior to any data collection			
FDh maximum value			
FEh value is not valid			
FFh invalid for attribute value – not to be used			
Vendor Specific	8	04h	binary
Total Bytes	12		

Figure 129. Individual Attribute Data Structure

12.31.2.2.1 Attribute ID Numbers: Any non-zero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers. Those marked with (*) indicate that corresponding Attribute Values can be collected only during off-line test.

ID	Attribute Name
0	Indicates that this entry in the data structure is not used
1	Raw Read Error Rate
2	Throughput Performance (*)
3	Spin Up Time
4	Start/Stop Count
5	Reallocated Sector Count
7	Seek Error Rate

8 Seek Time Performance (*)

9 Power-On Hours Count

10 Spin Retry Count

12 Device Power Cycle Count

197 Current Pending Sector Count

198 Off-Line Scan Uncorrectable Sector Count

199 Ultra DMA CRC Error Count

12.31.2.2.2 Status Flag Definitions

Bit	Flag Name	Definition
0	Pre–Failure/ Advisory bit	If bit = 0, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates an Advisory condition where the usage or age of the device has exceeded its intended design life period. If bit = 1, an Attribute Value less than or equal to its corresponding Attribute Threshold indicates a Pre–Failure condition where imminent loss of data is being predicted.
1	On–Line Collective bit	If bit = 0, the Attribute Value is updated only during Off–Line testing. If bit = 1, the Attribute Value is updated during On–Line testing or during both On–Line and Off–Line testing.
2– 5	Vendor Specific	
6–15	Reserved bits	Always 0

Figure 130. Status Flag Definitions

12.31.2.2.3 Normalized Values: The device will perform conversion of the raw Attribute Values to transform them into normalized values, which the host can then compare with the Threshold values. A Threshold is the excursion limit for a normalized Attribute Value. In normalizing the raw data, the device will perform any necessary statistical validity checks to ensure that an instantaneous raw value is not improperly reflected in the normalized Attribute Value (i.e., one read error in the first 10 reads being interpreted as exceeding the read error rate threshold when the subsequent 1 billion reads all execute without error). The end points for the normalized values for all Attributes will be 1 (01h) at the low end, and 100 (64h) at the high end for the device which is ready for customer shipment. For Performance and Error Rate Attributes, values greater than 100 are also possible, up to a maximum value of 253 (FDh).

12.31.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates Automatic Off-Line Data Collection Status.

Bit 7	Automatic Off-Line Data Collection Status
1	Automatic Off-Line Data Collection is enabled.
0	Automatic Off-Line Data Collection is disabled.

Bits 0 thru 6 represents a hexadecimal status value reported by the device.

Value	Definition
0	Off-line data collection never started
1	Segment completed without error
2	All segments completed without errors. In this case, current segment pointer equals to total segments required.
4	Off-line data collecting suspended by interrupting command
5	Off-line data collecting aborted by interrupting command
6	Off-line data collection aborted with fatal error

12.31.2.4 Total Segments Required for Off-line Data Collection

The device will return 01h as the total segments for off-line data collection.

12.31.2.5 Total Time in Seconds to Complete Off-line Data Collection Activity

This field tells the host how many seconds the device requires to complete the segment pointed by the current segment pointer. The host can use this time to set a count down timer that will trigger it to issue the "SMART Read Attribute Values" subcommand to check on the status of off-line data collection. This field indicates the total time in seconds for the first segment if the current segment pointer is 00h or the off-line status indicates all segments completed (02h).

12.31.2.6 Current Segment Pointer

This byte is a counter indicating the next segment to execute as an off-line data collection activity. This varies from 00h to the total number of segments. The current segment pointer will be 00h if the off-line data collection has not been started. If the off-line data collection is aborted by a command or an error (i.e., the status is 05h or 06h), this byte will point to the aborted segment. If the all segments complete, this byte will equal to the total number of segments.

12.31.2.7 Off-Line Data Collection Capability

The device returns 0Bh as its off-line data collection capability which indicates: the Execute Off-Line Data Collection Immediate is implemented; the Automatic Off-Line Data Collection is implemented; the Off-Line Read Scanning with Defect Reallocation is implemented.

12.31.2.8 S.M.A.R.T. Capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit	Definition
0	Pre-power mode attribute saving capability If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).
1	Attribute autosave capability If bit = 1, the device supports the SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.
2-15	Reserved (0)

12.31.2.9 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

12.31.3 Device Attribute Thresholds Data Structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the SMART Read Attribute Thresholds. All multi-byte fields shown in these data structures follow the ATA/ATAPI-4 specifications for byte ordering, namely that the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

Description	Bytes	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0005h
1st Attribute Threshold	12	02h	(*1)	(*2)
...	..			
...	..			
30th Attribute Threshold	12	15Eh	(*1)	(*2)
Reserved	18	16Ah		(*3)
Vendor specific	131	17Ch		(*3)
Data structure checksum	1	1FFh		(*2)
	512			

(*1) – See following definitions
(*2) – Value varied by actual operating condition
(*3) – Filled with 00h

Figure 131. Device Attribute Thresholds Data Structure

12.31.3.1 Data Structure Revision Number

This value (0005h) is the same as the value used in the Device Attributes Values Data Structure.

12.31.3.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure is in the same order and correspond to the entries in the Individual Attribute Data Structure.

Description	Bytes	Offset	Format
Attribute ID Number (01h to FFh)	1	00h	binary
Attribute Threshold (for comparison with Attribute Values from 00h to FFh)	1	01h	binary
00h – "always passing" threshold value to be used for code test purposes			
01h – minimum value for normal operation			
FDh – maximum value for normal operation			
FEh – invalid for threshold value			
FFh – "always failing" threshold value to be used for code test purposes			
Reserved (00h)	10	02h	binary
Total Bytes	12		

Figure 132. Individual Threshold Data Structure

12.31.3.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

12.31.3.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable.

12.31.3.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

12.31.4 Error Reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

Error Condition	Status Register	Error Register
A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the Cylinder High and Cylinder Low registers.	51h	04h
A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A S.M.A.R.T. FUNCTION SET command subcommand other than SMART ENABLE OPERATIONS was received by the device while the device was in a "S.M.A.R.T. disabled" state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure.	51h	10h or 40h
The device is unable to write to its Attribute Values data structure.	51h	10h or 01h
The Data Structrue Revision Number in the device's Attribute Values data structure does not match the Data Structure Revision Number in the device's Attribute Thresholds data structure.	51h	01h
A mismatch has occurred between the entries in the device's Attribute Values data structure and Attribute Thresholds data structure.	51h	01h
The device has detected a checksum error in its Attribute Threshold data structure.	51h	10h

Figure 133. S.M.A.R.T. Error Codes

12.32 Standby (E2h/96h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 0 0 1 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 134. Standby Command (E2h/96h)

The Standby command causes the device to enter the Standby Mode immediately, and set auto power down timeout parameter(standby timer).

When the Standby mode is entered, the drive is spun down but the interface remains active. If the drive is already spun down, the spin down sequence is not executed.

During the Standby mode the drive will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The automatic power down sequence is enabled and the timer starts counting down when the drive returns to Idle mode.

Output Parameters To The Drive

Sector Count Timeout Parameter. If zero, then the automatic power down sequence is disabled. If non-zero,then the automatic power down sequence is enabled,and the timeout interval is shown blow:

Value	Timeout
0	Timer disabled
1 - 240	Value * 5 seconds
241 - 251	(Value-240) * 30 minutes
252	21 minutes
253	8 hours
254	21 minutes 10 seconds
255	21 minutes 15 seconds

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the timeout interval expires with no drive access from the host. The timeout interval will be reinitialized if there is a drive access before the timeout interval expires.

12.33 Standby Immediate (E0h/94h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 0 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 135. Standby Immediate Command (E0h/94h)

The Standby Immediate command causes the device to enter Standby mode immediately.

The device is spun down but the interface remains active. If the device is already spun down, the spin down sequence is not executed.

During the Standby mode, the device will respond to commands, but there is a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect to auto power down timeout parameter.

12.34 Write Buffer (E8h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	1 – 1 D – – – –
Command	1 1 1 0 1 0 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – –
Sector Number	– – – – – – – –
Cylinder Low	– – – – – – – –
Cylinder High	– – – – – – – –
Device/Head	– – – – – – – –
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	0	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	–	–	0	–	V

Figure 136. Write Buffer Command (E8h)

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within buffer.

12.35 Write DMA (CAh/CBh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 1 0 1 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN
0	0	0	V	0	V	0	0

Status Register							
7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	V	V	–	0	–	V

Figure 137. Write DMA Command (CAh/CBh)

The Write DMA command transfers one or more sectors of data from the host to the device, then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.)

Input Parameters From The Device

Sector Count The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number The sector number of the last transferred sector. (L=0)

In LBA mode, this register contains current LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the last transferred sector. (L=0)

In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the last transferred sector. (L=0)

In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.36 Write DMA Queued (CCh)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	V V V V V V V V
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 1 1 0 0

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
V	0	0	V	0	V	0	V

Status Register							
7 BSY	6 RDY	5 DF	4 SRV	3 DRQ	2 COR	1 IDX	0 ERR
0	V	0	V	–	0	–	V

Figure 138. Write DMA Queued Command (CCh)

This command executes in a similar manner to a WRITE DMA command. The device may perform a bus release or it may execute the data transfer without performing a bus release if the data is ready to transfer.

If the device performs a bus release, the host shall reselect the device using the SERVICE command.

Once the data transfer is begun, the device does not perform a bus release until the entire data transfer has been completed.

Output Parameters To The Device

Feature number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Count bits 7 - 3 (Tag) contain the Tag for the command being delivered.

Sector Number starting sector number or LBA address bits 7 - 0.

Cylinder High/Low starting cylinder number or LBA address bits 23 - 8.

H starting head number or LBA address bits 27 - 24.

Input Parameters From The Device On Bus Release

Sector Count bits 7 - 3 (Tag) contain the Tag of the command being bus released.

bit 2 (REL) is set to one.

bit 1 (I/O) is cleared to zero.

bit 0 (C/D) is cleared to zero.

Sector Number, Cylinder High/Low, H n/a.

SRV cleared to zero when the device performs a bus release. This bit is set to one when the device is ready to transfer data.

Input Parameters From The Device On Command Complete

Sector Count bits 7 - 3 (Tag) contain the Tag of the completed command.

bit 2 (REL) is cleared to zero.

bit 1 (I/O) is set to one.

bit 0 (C/D) is set to one.

Sector Number, Cylinder High/Low, H sector address of unrecoverable error. (applicable only when unrecoverable error has occurred.)

SRV cleared to zero.

12.37 Write Long (32h/33h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	0 0 0 0 0 0 0 1
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 1 0 0 1 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	– – – – – – – V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	V	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	V	V	–	0	–	V

Figure 139. Write Long Command (32h/33h)

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, then the data and the ECC bytes are written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ=1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time, and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 34 according to setting of Set Feature option. The default number after power on is 4 bytes.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number The sector number of the sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled.

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred.
Sector Number	The sector number of the sector to be transferred. (L=0)
	In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the sector to be transferred. (L=0)
	In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the sector to be transferred. (L=0)
	In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

The file internally uses 34 bytes of ECC on all data read or writes. The 4 byte mode of operation is provided via an emulation technique. As a consequence of this emulation it is recommended that 34 byte ECC mode is used for all tests to confirm the operation of the files ECC hardware. Unexpected results may occur if such testing is performed using 4 byte mode.

12.38 Write Multiple (C5h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	1 1 0 0 0 1 0 1

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	V	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	V	V	–	0	–	V

Figure 140. Write Multiple Command (C5h)

The Write Multiple command transfers one or more sectors from the host to the device, the the data is written to the disk media.

Command execution is identical to the Write Sectors command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

12.39 Write Sectors (30h/31h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Feature	– – – – – – – –
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H
Command	0 0 1 1 0 0 0 R

Command Block Input Registers	
Register	7 6 5 4 3 2 1 0
Data	– – – – – – – –
Error	...See Below...
Sector Count	V V V V V V V V
Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V
Device/Head	– – – – H H H H
Status	...See Below...

Error Register							
7 CRC	6 UNC	5 0	4 IDN	3 0	2 ABT	1 T0N	0 AMN
0	0	0	V	0	V	0	0

Status Register							
7 BSY	6 RDY	5 DF	4 DSC	3 DRQ	2 COR	1 IDX	0 ERR
0	V	V	V	–	0	–	V

Figure 141. Write Sectors Command (30h/31h)

The Write Sectors command transfers one or more sectors from the host to the device, then the data is written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output Parameters To The Device

Sector Count The number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number The sector number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 0 - 7. (L=1)

Cylinder High/Low The cylinder number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)

H The head number of the first sector to be transferred. (L=0)

In LBA mode, this register contains LBA bits 24 - 27. (L=1)

R The retry bit. If set to one, then retries are disabled. But ignored, when write cache is enabled. (Ignoring the retry bit is in violation of ATA-2.)

Input Parameters From The Device

Sector Count	The number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.
Sector Number	The sector number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 0 - 7. (L=1)
Cylinder High/Low	The cylinder number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 8 - 15 (Low), 16 - 23 (High). (L=1)
H	The head number of the last transferred sector. (L=0)
	In LBA mode, this register contains current LBA bits 24 - 27. (L=1)

13.0 Timeout Values

The timing of BSY and DRQ in Status Register are shown in Figure 142.

FUNCTION	INTERVAL	START	STOP	TIMEOUT
Power On	Device Busy After Power On	Power On	Status Register BSY=1	400 ns
	Device Ready After Power On	Power On	Status Register BSY=0 and RDY=1	31 sec
Software Reset	Device Busy After Software Reset	Device Control Register RST=1	Status Register BSY=1	400 ns
	Device Ready After Software Reset	Device Control Register RST=0 After RST = 1	Status Register BSY=0 and RDY=1	31 sec
Hard Reset	Device Busy After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=1	400 ns
	Device Ready After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=0 and RDY=1	31 sec
Data In Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt, DRQ For Data Transfer In	Status Register BSY=1	Status Register BSY=0 and DRQ=1, Interrupt	30 sec
	Device Busy After Data Transfer In	256th Read From Data Register	Status Register BSY=1	10 us
Data Out Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Data Request For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and DRQ=1	700 us
	Device Busy After Data Transfer Out	256th Write From Data Register	Status Register BSY=1	5 us
	Interrupt For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and RDY=1 Interrupt	30 sec

Figure 142. Timeout Values

FUNCTION	INTERVAL	START	STOP	TIMEOUT
Non—Data Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt For Command Complete	Status Register BSY=1	Interrupt	30 sec
DMA Data Transfer Command	Device Busy after Command Code Out	Out to Command Register	Status Register BSY=1	400 ns

Figure 143. Timeout Values --- Continued ---

Command category is referred to 11.0, “Command Protocol” on page 101.

The abbreviations "ns", "us", "ms" and "sec" mean nanoseconds, microseconds, milliseconds and seconds, respectively.

We recommend that the host system executes Soft reset and then retry to issue the command if the host system would occur timeout for the device.

14.0 Appendix

14.1 Commands Support Coverage

Following table is provided to facilitate the understanding of DJNA-3xxxxx command support coverage comparing to the ATA/ATAPI-4 defined command set. The column of 'Implementation' shows the capability of DJNA-3xxxxx for those commands.

Command Code	Command Name	Implementation for DJNA–3XXXXX	ATA–4 Command Type
00h	NOP	Yes	Optional
01h–07h	Reserved	Reserved	Reserved
08h	DEVICE RESET	No	Optional
09h–0Fh	Reserved	Reserved	Reserved
10h	RECALIBRATE	Yes	Obsolete
11h–1Fh	RECALIBRATE	Yes	Retired
20h	READ SECTOR(S) (w/ retry)	Yes	Mandatory
21h	READ SECTOR(S) (w/o retry)	Yes	Mandatory
22h	READ LONG (w/ retry)	Yes	Obsolete
23h	READ LONG (w/o retry)	Yes	Obsolete
24h–2Fh	Reserved	Reserved	Reserved
30h	WRITE SECTOR(S) (w/ retry)	Yes	Mandatory
31h	WRITE SECTOR(S) (w/o retry)	Yes	Mandatory
32h	WRITE LONG (w/ retry)	Yes	Obsolete
33h	WRITE LONG (w/o retry)	Yes	Obsolete
34h–3Bh	Reserved	Reserved	Reserved
3Ch	WRITE VERIFY	No	Obsolete
3Dh–3Fh	Reserved	Reserved	Reserved
40h	READ VERIFY SECTOR(S) (w/ retry)	Yes	Mandatory
41h	READ VERIFY SECTOR(S) (w/o retry)	Yes	Mandatory
42h–4Fh	Reserved	Reserved	Reserved
50h	FORMAT TRACK	Yes	Obsolete
51h–5Fh	Reserved	Reserved	Reserved
60h–6Fh	Reserved	Reserved	Reserved
70h	SEEK	Yes	Mandatory
71h–7Fh	SEEK	Yes	Retired
8xh	Vendor specific	Reserved	Vendor specific
90h	EXECUTE DEVICE DIAGNOSTIC	Yes	Mandatory
91h	INITIALIZE DEVICE PARAMETERS	Yes	Mandatory
92h	DOWNLOAD MICROCODE	No	Optional
93h	Reserved	Reserved	Reserved
94h	STANDBY IMMEDIATE (1)	Yes	Retired (2)
95h	IDLE IMMEDIATE (1)	Yes	Retired (2)
96h	STANDBY (1)	Yes	Retired (2)
97h	IDLE (1)	Yes	Retired (2)
98h	CHECK POWER MODE (1)	Yes	Retired (2)
99h	SLEEP (1)	Yes	Retired (2)
9Ah	Vendor specific	Reserved	Vendor specific
9Bh–9Fh	Reserved	Reserved	Reserved
A0h	PACKET	No	Optional
A1h	IDENTIFY PACKET DEVICE	No	Optional
A2h	SERVICE	Yes	Optional
A0h–AFh	Reserved	Reserved	Reserved
B0h	SMART FUNCTION SET	Yes	Optional – (4)

Figure 144. Command coverage

Command Code	Command Name	Implementation for DJNA-3XXXXX	ATA-4 Command Type
B1h-BFh	Reserved	Reserved	Reserved
C0h-C3h	Vendor specific	Reserved	Vendor specific
C4h	READ MULTIPLE	Yes	Mandatory
C5h	WRITE MULTIPLE	Yes	Mandatory
C6h	SET MULTIPLE MODE	Yes	Mandatory
C7h	READ DMA QUEUED	Yes	Optional
C8h	READ DMA (w/ retry)	Yes	Mandatory
C9h	READ DMA (w/o retry)	Yes	Mandatory
CAh	WRITE DMA (w/ retry)	Yes	Mandatory
CBh	WRITE DMA (w/o retry)	Yes	Mandatory
CCh	WRITE DMA QUEUED	Yes	Optional
CDh-CFh	Reserved	Reserved	Reserved
D0h-D9h	Reserved	Reserved	Reserved
DAh	GET MEDIA STATUS	No	Optional - (5)
DBh-DDh	Reserved	Reserved	Retired
DEh	MEDIA LOCK	No	Optional - (5)
DFh	MEDIA UNLOCK	No	Optional - (5)
E0h	STANDBY IMMEDIATE (1)	Yes	Optional - (2)
E1h	IDLE IMMEDIATE (1)	Yes	Optional - (2)
E2h	STANDBY (1)	Yes	Optional - (2)
E3h	IDLE (1)	Yes	Optional - (2)
E4h	READ BUFFER	Yes	Optional
E5h	CHECK POWER MODE (1)	Yes	Optional - (2)
E6h	SLEEP (1)	Yes	Optional - (2)
E7h	FLUSH CACHE	Yes	Optional
E8h	WRITE BUFFER	Yes	Optional
E9h	WRITE SAME	No	Retired
EAh-EBh	Reserved	Reserved	Reserved
ECh	IDENTIFY DEVICE	Yes	Mandatory
EDh	MEDIA EJECT	No	Optional - (5)
EEh	IDENTIFY DEVICE DMA	No	Obsolete
EFh	SET FEATURES	Yes	Optional
F0h	Vendor specific	Reserved	Vendor specific
F1h	SET PASSWORD (3)	Yes	Optional
F2h	UNLOCK (3)	Yes	Optional
F3h	ERASE PREPARE (3)	Yes	Optional
F4h	ERASE UNIT (3)	Yes	Optional
F5h	FREEZE LOCK (3)	Yes	Optional
F6h	DISABLE PASSWORD (3)	Yes	Optional
F7h	Vendor specific	Reserved	Vendor specific
F8h	READ NATIVE MAX LBA/CYL	Yes	Optional
F9h	SET MAX LBA/CYL	Yes	Optional
FAh-FFh	Vendor specific	Reserved	Vendor specific

Note:(1) These commands have two command codes and appear in this table twice, once for each command code.
(2) Power Management Feature Set
(3) Secure Mode Feature Set
(4) S.M.A.R.T. Function Set
(5) Removable

Figure 145. Command coverage --- Continued ---

14.2 SET FEATURES Command Support Coverage

Following table is provided to facilitate the understanding of DJNA-3xxxxx "Set Features" command support coverage comparing to the ATA/ATAPI-4 defined command set. The column of 'Implementation' shows the capability of DJNA-3xxxxx for those commands. For detail operation, refer to 12.27, “Set Features (EFh)” on page 153.

Features Register	Features Name	Implementation for DJNA–3XXXXX	ATA–4 Command Type
01h	Enable 8 bit data transfers	No	Retired
02h	Enable write cache	Yes	Mandatory
03h	Set transfer mode	Yes	Mandatory
04h	Enable all auto reassignment	No	Obsolete
05h	Enable advanced power management	No	Optional
09h	Enable Address Offset mode	Yes	Reserved
31h	Disable Media Status Notification	No	Optional
33h	Disable retry	No	Obsolete
44h	Set vendor specific bytes ECC	Yes	Obsolete
54h	Set cache segments	No	Obsolete
55h	Disable read look–ahead feature	Yes	Optional
5Dh	Enable release interrupt	Yes	Optional
5Eh	Enable SERVICE interrupt	No	Optional
66h	Disable reverting to power on defaults	Yes	Optional
77h	Disable ECC	No	Obsolete
81h	Disable 8 bit data transfers	No	Retired
82h	Disable write cache	Yes	Mandatory
84h	Disable all auto reassignment	No	Obsolete
85h	Disable advanced power management	No	Optional
88h	Enable ECC	No	Obsolete
89h	Disable Address Offset mode	Yes	Reserved
95h	Enable Media Status Notification	No	Optional
99h	Enable retries	No	Obsolete
9Ah	Set device maximum average current	No	Obsolete
AAh	Enable read look–ahead feature	Yes	Optional
ABh	Set maximum prefetch	No	Obsolete
BBh	Set 4 bytes ECC	Yes	Obsolete
CCh	Enable reverting to power on defaults	Yes	Optional
DDh	Disable release interrupt	Yes	Optional
DEh	Disable SERVICE interrupt	No	Optional
others	Reserved	Reserved	Reserved

Figure 146. SET FEATURES Command coverage

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