HITACHI
Inspire the Next

Hard Disk Drive Specification

Deskstar 7K250

3.5 inch Ultra ATA/100 hard disk drive

Models: HDS722525VLAT80
HDS722516VLAT80
HDS722516VLAT20
HDS722512VLAT80
HDS722512VLAT20
HDS722580VLAT20
HDS722540VLAT20

Version 1.4

21 September 2005

HITACHI
Inspire the Next

Hard Disk Drive Specification

Deskstar 7K250

3.5 inch Ultra ATA/100 hard disk drive

Models: HDS722525VLAT80
HDS722516VLAT80
HDS722516VLAT20
HDS722512VLAT80
HDS722512VLAT20
HDS722580VLAT20
HDS722540VLAT20

Version 1.4

21 September 2005

1st Edition (Revision 0.1) Sxxx-xxxx-01 (1 April 2003) Preliminary
2nd Edition (Revision 0.2) Sxxx-xxxx-01 (5 June 2003) Revision
3rd Edition (Revision 0.3) Sxxx-xxxx-03 (8 July 2003) Revision
4th Edition (Revision 1.0) Sxxx-xxxx-10 (14 July 2003) Revision
5th Edition (Revision 1.1) Sxxx-xxxx-11 (13 August 2003) Revision
6th Edition (Revision 1.2) (09 February 2004) Revision
7th Edition (Revision 1.3) (24 June2004) Revision
8th Edition (Revision 1.4) (21 September 2005) Final

Table Of Contents

1.0 General....1

1.1 Introduction....1
1.2 References....1
1.3 Abbreviations....1
1.4 Caution....3

2.0 General features of the drive....5

3.0 Fixed-disk subsystem description....9

3.1 Control electronics....9
3.2 Head disk assembly....9
3.3 Actuator....9

4.0 Drive characteristics....11

4.1 Default logical drive parameters....11
4.2 Data sheet....12
4.3 Drive organization....13
4.3.1 Drive format....13
4.3.2 Cylinder allocation....13
4.4 Performance characteristics....15
4.4.1 Command overhead....15
4.4.2 Mechanical positioning....15
4.4.3 Drive ready time....17
4.4.4 Data transfer speed....18
4.4.5 Throughput....19
4.4.6 Operating modes....20

5.0 Defect flagging strategy....21

6.0 Specification....23

6.1 Jumper settings....23
6.1.1 Jumper pin location....23
6.1.2 Jumper pin identification....23
6.1.3 Jumper pin assignment....24
6.1.4 Jumper positions....24
6.2 Environment....28
6.2.1 Temperature and humidity....28
6.2.2 Corrosion test....29
6.3 DC power requirements....29
6.3.1 Input voltage....29

6.3.2 Power supply current (typical) 29
6.3.3 Power supply generated ripple at drive power connector 31
6.4 Reliability 32
6.4.1 Data integrity 32
6.4.2 Cable noise interference 32
6.4.3 Start/stop cycles 32
6.4.4 Preventive maintenance 32
6.4.5 Data reliability 32
6.4.6 Required power-off sequence 32
6.5 Mechanical specifications 33
6.5.1 Physical dimensions and weight 33
6.5.2 Mounting hole locations 34
6.5.3 Connector locations 35
6.5.4 Drive mounting 35
6.5.5 Heads unload and actuator lock 35
6.6 Vibration and shock 36
6.6.1 Operating vibration 36
6.6.2 Nonoperating vibration 36
6.6.3 Operating shock 37
6.6.4 Nonoperating shock 37
6.6.5 Nonoperating rotational shock 38
6.7 Acoustics 39
6.8 Identification labels 39
6.9 Safety 40
6.9.1 UL and CSA approval 40
6.9.2 German safety mark 40
6.9.3 Flammability 40
6.9.4 Safe handling 40
6.9.5 Environment 40
6.9.6 Secondary circuit protection 40
6.10 Electromagnetic compatibility 41
6.10.1 CE mark 41
6.10.2 C-TICK mark 41
6.10.3 BSMI mark 41
6.11 Packaging 41

7.0 Electrical interface specification 43

7.1 Connector location 43
7.1.1 DC power connector 43
7.1.2 AT signal connector 43
7.2 Signal definitions 44
7.3 Signal descriptions 45
7.4 Interface logic signal levels 48
7.5 Reset timings 48
7.6 PIO timings 49
7.6.1 Write DRQ interval time 49

7.6.2 Read DRQ interval time 50
7.7 Multi word DMA timings 51
7.8 Ultra DMA timings 52
7.8.1 Initiating Read DMA 52
7.8.2 Host Pausing Read DMA 53
7.8.3 Host Terminating Read DMA 54
7.8.4 Device Terminating Read DMA 55
7.8.5 Initiating Write DMA 56
7.8.6 Device Pausing Write DMA 57
7.8.7 Device Terminating Write DMA 58
7.8.8 Host Terminating Write DMA 59
7.9 Addressing of registers 60
7.9.1 Cabling 60

8.0 General 63

8.1 Introduction 63
8.2 Terminology 63
8.3 Deviations from standard 63

9.0 Registers 65

9.1 Register set 65
9.2 Alternate Status Register 66
9.3 Command Register 66
9.4 Cylinder High Register 66
9.5 Cylinder Low Register 66
9.6 Data Register 67
9.7 Device Control Register 67
9.8 Drive Address Register 68
9.9 Device/Head Register 68
9.10 Error Register 69
9.11 Features Register 69
9.12 Sector Count Register 69
9.13 Sector Number Register 70
9.14 Status Register 70

10.0 General operation 73

10.1 Reset response 73
10.2 Register initialization 74
10.3 Diagnostic and Reset considerations 75
10.4 Sector Addressing Mode 76
10.4.1 Logical CHS addressing mode 76
10.4.2 LBA addressing mode 76
10.5 Overlapped and queued feature 76
10.6 Power management features 78
10.6.1 Power mode 78

10.6.2 Power management commands 78
10.6.3 Standby timer 78
10.6.4 Interface capability for power modes 79
10.7 S.M.A.R.T. Function 80
10.7.1 Attributes 80
10.7.2 Attribute values 80
10.7.3 Attribute thresholds 80
10.7.4 Threshold exceeded condition 80
10.7.5 S.M.A.R.T. commands 80
10.7.6 Off-line read scanning 80
10.7.7 Error log 81
10.7.8 Self-test 81
10.8 Security Mode Feature Set 82
10.8.1 Security mode 82
10.8.2 Security level 82
10.8.3 Passwords 83
10.8.4 Operation example 83
10.8.5 Command table 86
10.9 Host Protected Area Feature 87
10.9.1 Example for operation (In LBA Mode) 87
10.9.2 Security extensions 88
10.10 Seek overlap 89
10.11 Write cache function 90
10.12 Reassign function 91
10.12.1 Auto Reassign function 91
10.13 Power-Up in Standby feature set 92
10.14 Advanced Power Management feature set (APM) 93
10.15 Automatic Acoustic Management feature set (AAM) 94
10.16 Address Offset Feature 95
10.16.1 Enable/Disable Address Offset Mode 95
10.16.2 Identify Device Data 96
10.16.3 Exceptions in Address Offset Mode 96
10.17 48-bit Address Feature Set 97

11.0 Command protocol 99

11.1 PIO Data In commands 99
11.2 PIO Data Out Commands 100
11.3 Non-data commands 102
11.4 DMA commands 103
11.5 DMA queued commands 104

12.0 Command descriptions 105

12.1 Check Power Mode (E5h/98h) 109
12.2 Device Configuration Overlay (B1h) 110
12.2.1 DEVICE CONFIGURATION RESTORE 110

12.2.2 DEVICE CONFIGURATION FREEZE LOCK (subcommand C1h)110
12.2.3 DEVICE CONFIGURATION IDENTIFY (subcommand C2h).111
12.2.4 DEVICE CONFIGURATION SET (subcommand C3h) 111
12.3 Execute Device Diagnostic (90h) 114
12.4 Flush Cache (E7h) 115
12.5 Flush Cache Ext (EAh) 116
12.6 Format Track (50h) 117
12.7 Format Unit (F7h) 118
12.8 Identify Device (ECh) 119
12.9 Idle (E3h/97h) 127
12.10 Idle Immediate (E1h/95h) 128
12.11 Initialize Device Parameters (91h) 129
12.12 NOP (00h) 130
12.13 Read Buffer (E4h) 131
12.14 Read DMA (C8h/C9h) 132
12.15 Read DMA Ext (25h) 134
12.16 Read DMA Queued (C7h) 136
12.17 Read DMA Queued Ext (26h) 138
12.18 Read Log Ext (2Fh) 140
12.18.1 General Purpose Log Directory 141
12.18.2 Extended Comprehensive SMART Error Log.....142
12.18.3 Extended Self-test log sector 144
12.19 Read Long (22h/23h) 146
12.20 Read Multiple (C4h) 148
12.21 Read Multiple Ext (29h) 150
12.22 Read Native Max ADDRESS (F8h) 152
12.23 Read Native Max Address Ext (27h) 153
12.24 Read Sectors (20h/21h) 154
12.25 Read Sector(s) Ext (24h) 156
12.26 Read Verify Sectors (40h/41h) 158
12.27 Read Verify Sector(s) (42h) 160
12.28 Recalibrate (1xh) 162
12.29 Security Disable Password (F6h) 163
12.30 Security Disable Password (F3h) 164
12.31 Security Erase Unit (F4h) 165
12.32 Security Freeze Lock (F5h) 167
12.33 Security Set Password (F1h) 168
12.34 Security Unlock (F2h) 170
12.35 Seek (7xh) 171
12.36 Service (A2h .....)172
12.37 Set Features (EFh) 173
12.37.1 Set Transfer mode 174
12.37.2 Write Cache 174
12.37.3 Advanced Power Management 174
12.37.4 Automatic Acoustic Management 175
12.38 Set Max ADDRESS (F9h) 176

12.38.1 Set Max Set Password (Feature=01h)....178
12.38.2 Set Max Lock (Feature=02h)....179
12.38.3 Set Max Unlock (Feature = 03h)....180
12.38.4 Set Max Freeze Lock (Feature = 04h)....181
12.39 Set Max Address Ext (37h)....182
12.40 Set Multiple (C9h)....184
12.41 Sleep (E6h/99h)....185
12.42 S.M.A.R.T. Function Set (B0h)....186
12.42.1 S.M.A.R.T. Function Subcommands....186
12.42.2 Device Attribute Data Structure....190
12.42.3 Device Attribute Thresholds data structure....193
12.42.4 S.M.A.R.T. Log Directory....195
12.42.5 S.M.A.R.T. summary error log sector....195
12.42.6 Self-test log data structure....197
12.42.7 Error reporting....198
12.43 Standby (E2h/96h)....199
12.44 Standby Immediate (E0h/94h)....200
12.45 Write Buffer (E8h)....201
12.46 Write DMA (CAh/CBh)....202
12.47 Write DMA Ext (35h)....204
12.48 Write DMA Queued (CAh/CBh)....206
12.49 Write DMA Queued Ext (36h)....208
12.50 Write Log Ext (3Fh)....210
12.51 Write Long (32h/33h)....211
12.52 Write Multiple (C5h)....213
12.53 Write Multiple Ext (39h)....215
12.54 Write Sectors (30h/31h)....217
12.55 Write Sector(s) (34h)....219

13.0 Time-out values....221

List of Tables

Table 1.Formatted capacities 11
Table 2.Mechanical positioning performance 12
Table 3.Cylinder allocation 13
Table 4.Command overhead 15
Table 5.Mechanical positioning performance 15
Table 6.Full stroke seek time 16
Table 7.Head switch time 16
Table 8.Single track seek time 17
Table 9.Latency Time 17
Table 10.Drive ready time 17
Table 11.Data transfer speed 18
Table 12.Simple Sequential Access performance 19
Table 13.Random Access performance 19
Table 14.Random Access Performance 19
Table 15.Description of operating modes 20
Table 16.Mode transition time 20
Table 17.Plist physical format 21
Table 18.Jumper positions for capacity clip to 2GB/32GB 26
Table 19.Jumper settings for Disabling Auto Spin 26
Table 20.Temperature and humidity 28
Table 21.Input voltage 29
Table 22.Power supply current of xxx-GB models 29
Table 23.Power supply generated ripple at drive power connector 31
Table 24.Random vibration PSD 36
Table 25.Random vibration PSD profile break points (operating) 36
Table 26.Random Vibration PSD profile breakpoints (nonoperating) 36
Table 27.Sinusoidal shock wave 38
Table 28.Rotational shock 38
Table 29.Sound power levels 39
Table 30.Sound power levels 39
Table 31.Signal definitions 44
Table 32.Special signal definitions for Ultra DMA 45
Table 33.I/O address map 60
Table 34.Register Set 65
Table 35.Alternate Status Register 66
Table 36.Device Control Register 67
Table 37.Drive Address Register 68
Table 38.Device Head/Register 68
Table 39.Error Register 69
Table 40.Status Register 70
Table 41.Reset response table 73

Table 42.Default Register Values 74
Table 43.Diagnostic codes 74
Table 44.Reset error register values 75
Table 45.Power conditions 79
Table 46.Command table for device lock operation 86
Table 47.Command Set (1 of 2) 105
Table 48.Command Set (2 of 2) 106
Table 49.Command Set (subcommand) 107
Table 50.Check Power Mode command (E5h/98h) 109
Table 51.Check Power Mode Command (E5h/98h) 110
Table 52.Device Configuration Overlay Features register values 110
Table 53.Device Configuration Overlay Data structure 112
Table 54.DCO error information definition 113
Table 55.Execute Device Diagnostic command (90h) 114
Table 56.Flush Cache command (E7h) 115
Table 57.Flush Cache Ext Command (EAh) 116
Table 58.Format Track command (50h) 117
Table 59.Format Unit command (F7h) 118
Table 60.Identify Device command (ECh) 119
Table 61.Identify device information (Part 1 of 7) 120
Table 62.Identify device information (Part 2 of 7) 121
Table 63.Identify device information (Part 3 of 7) 122
Table 64.Identify device information (Part 4 of 7) 123
Table 65.Identify device information (Part 5 of 7 124
Table 66.Identify device information (Part 6 of 7) 125
Table 67.Identify device information (Part 7 of 7) 126
Table 68.Idle command (E3h/97h) 127
Table 69.Idle Immediate command (E1h/95h) 128
Table 70.Initialize Device Parameters command (91h) 129
Table 71.NOP Command (00h) 130
Table 72.Read Buffer (E4h) 131
Table 73.Read DMA command (C8h/C9h) 132
Table 74.Read DMA Ext Command (25h) 134
Table 75.Read DMA command (C8h/C9h) 136
Table 76.Read DMA Ext Command (25h) 138
Table 77.Read Log Ext Command (2Fh) 140
Table 78.Log Address Definition 141
Table 79.General Purpose Log Directory 141
Table 80.Extended Comprehensive SMART Error Log 142
Table 81.Extended Error log data structure 142
Table 82.Command data structure 143
Table 83.Error data structure 143
Table 84.Read Long (22h/23h) 146
Table 85.Read Multiple (C4h) 148
Table 86.Read DMA Ext Command (25h) 150
Table 87.Read Native Max ADDRESS (F8h) 152

Table 88.Read Native Max Address Ext command (27h) 153
Table 89.Read Sectors Command (20h/21h) 154
Table 90.Read Sector(s) Ext command (24h) 156
Table 91.Read Verify Sectors (40h/41h) 158
Table 92.Read Verify Sector(s) command (42h) 160
Table 93.Recalibrate (1xh) 162
Table 94.Security Disable Password (F6h) 163
Table 95.Password Information for Security Disable Password command 163
Table 96.Security Disable Password (F3h) 164
Table 97.Security Erase Unit (F4h) 165
Table 98.Erase Unit information 165
Table 99.Security Freeze Lock command (F5h) 167
Table 100.Security Set Password command (F1h) 168
Table 101.Security Set Password Information 168
Table 102.Security Unlock command (F2h) 170
Table 103.Seek command (7xh) 171
Table 104.Service command (A2h) 172
Table 105.Set Features command (EFh) 173
Table 106.Set Max ADDRESS command (F9h) 176
Table 107.Set Max Set Password command 178
Table 108.Set Max Set Password data contents 178
Table 109.Set Max Lock command 179
Table 110.Set Max Unlock command (F9h) 180
Table 111.Set Max Freeze Lock (F9h) 181
Table 112.Set Max Address Ext command (37h) 182
Table 113.Set Multiple command (C6h) 184
Table 114.Sleep command (E6h/99h) 185
Table 115.S.M.A.R.T. Function Set command (B0h) 186
Table 116.Device Attribute Data Structure 190
Table 117.Individual Attribute Data Structure 190
Table 118.Device Attribute Thresholds Data Structure 194
Table 119.Individual Threshold Data Structure 194
Table 120.S.M.A.R.T. Log Directory 195
Table 121.S.M.A.R.T. summary error log sector 195
Table 122.Error log data structure 196
Table 123.Command data structure 196
Table 124.Error data structure 196
Table 125.Self-test log data structure 197
Table 126.S.M.A.R.T. Error Codes 198
Table 127.Standby (E2h/96h) 199
Table 128.Standby Immediate (E0h/94h) 200
Table 129.Write Buffer (E8h) 201
Table 130.Write DMA (CAh/CBh) 202
Table 131.Write DMA Ext Command (35h) 204
Table 132.Write DMA Queued Command CAh/CBh) 206
Table 133.Write DMA Queued Ext Command (36h) 208

Table 134.Write Log Ext Command (3Fh).....210
Table 135.Write Long (32h/33h).....211
Table 136.Write Multiple (C5h).....213
Table 137.Write Log Ext Command (3Fh).....215
Table 138.Write Sectors command (30h/31h).....217
Table 139.Write Sector(s) Command (34h).....219

1.0 General

1.1 Introduction

This document describes the specifications of the Deskstar 7K250, a 3.5-inch hard disk drive with ATA interface and a rotational speed of 7200 RPM.

HDS722540VLAT20	41.1GB
HDS722580VLAT20	82.3GB
HDS722512VLAT20/ HDS722512VLAT80	123.5GB
HDS722516VLAT20/ HDS722516VLA820	164.7GB
HDS722525VLAT80	250GB

These specifications are subject to change without notice.

1.2 References

- Information Technology - AT Attachment with Packet Interface-6.

1.3 Abbreviations

Abbreviation	Meaning
A	Ampere
AC	alternating current
AT	Advanced Technology
ATA	Advanced Technology Attachment
BIOS	Basic Input/Output System
C	Celsius
CSA	Canadian Standards Association
C-UL	Canadian-Underwriters Laboratory
Cyl	cylinder
DC	Direct Current
DFT	Drive Fitness Test
DMA	Direct Memory Access
ECC	error correction code
EEC	European Economic Community
EMC	electromagnetic compatibility
ERP	Error Recovery Procedure
ESD	Electrostatic Discharge
FCC	Federal Communications Commission

FRU	field replacement unit
G	gravity (a unit of force)
G^2/Hz	$(32\ ft/sec)^2$ per Hertz
Gb	1,000,000,000 bits
GB	1,000,000,000 bytes
GND	ground
h	hexadecimal
HDD	hard disk drive
Hz	Hertz
I	Input
ILS	integrated lead suspension
I/O	Input/Output
ISO	International Standards Organization
KB	1,000 bytes
Kbpi	1000 bits per inch
kgf-cm	kilogram (force)-centimeter
KHz	kilohertz
LBA	logical block addressing
Lw	unit of A-weighted sound power
m	meter
max	maximum
MB	1,000,000 bytes
Mbps	1,000,000 bits per second
MHz	megahertz
MLC	Machine Level Control
mm	millimeter
ms	millisecond
us, ms	microsecond
O	Output
OD	Open Drain Programmed Input/Output
PIO	
POH	power on hours
Pop	population
P/N	part number
p-p	peak-to-peak
PSD	power spectral density
RES	radiated electromagnetic susceptibility
RFI	radio frequency interference
RH	relative humidity
RMS	root mean square
RPM	revolutions per minute
RST	reset
R/W	read/write

sec	second
SELV	secondary low voltage
S.M.A.R.T	Self-Monitoring, Analysis, and Reporting Technology
TPI	tracks per inch
Trk	track
TTL	transistor-transistor logic
UL	Underwriters Laboratory
V	volt
VDE	Verband Deutscher Electrotechniker
W	watt
3-state	transistor-transistor tristate logic

1.4 Caution

- Do not apply force to the top cover.
- Do not cover the breathing hole on the top cover.
- Do not touch the interface connector pins or the surface of the printed circuit board
- This drive can be damaged by electrostatic discharge (ESD). Any damages incurred to the drive after its removal from the shipping package and the ESD protective bag are the responsibility of the user.

2.0 General features of the drive

- Formatted capacities of 40 GB - 250 GB
- Spindle speeds of 7200 RPM
- Fluid Dynamic Bearing motor
- Enhanced IDE interface
- Sector format of 512 bytes/sector
- Closed-loop actuator servo
- Load/Unload mechanism, non head disk contact start/stop
- Automatic Actuator lock
- Interleave factor 1:1
- Seek time of 8.5 ms (40-GB, 80-GB models), 8.2 ms (120GB, 160GB and 250GB) typical without Command Overhead
- Sector Buffer size of 2048 KB and 8192 KB (Upper 260 KB is used for firmware)
- Ring buffer implementation
- Write Cache
- Queued feature support
- Advanced ECC On The Fly (EOF)
- Automatic Error Recovery procedures for read and write commands
- Self Diagnostics on Power on and resident diagnostics
- PIO Data Transfer Mode 4 (16.6 MB/s)
- DMA Data Transfer
    - Multiword mode Mode 2 (16.6 MB/s)
    - Ultra DMA Mode 5 (100 MB/s)
- CHS and LBA mode
- Power saving modes/Low RPM idle mode (APM)
- S.M.A.R.T. (Self Monitoring and Analysis Reporting Technology)
- Support security feature
- Quiet Seek mode (AAM)
- 48-bit addressing feature

Part 1. Functional specification

3.0 Fixed-disk subsystem description

3.1 Control electronics

The drive is electronically controlled by a microprocessor, several logic modules, digital/analog modules, and various drivers and receivers. The control electronics performs the following major functions:

- Controls and interprets all interface signals between the host controller and the drive.
- Controls read write accessing of the disk media, including defect management and error recovery.
- Controls starting, stopping, and monitoring of the spindle.
- Conducts a power-up sequence and calibrates the servo.
- Analyzes servo signals to provide closed loop control. These include position error signal and estimated velocity.
- Monitors the actuator position and determines the target track for a seek operation.
- Controls the voice coil motor driver to align the actuator in a desired position.
- Constantly monitors error conditions of the servo and takes corresponding action if an error occurs.
- Monitors various timers such as head settle and servo failure.
- Performs self-checkout (diagnostics).

3.2 Head disk assembly

The head disk assembly (HDA) is assembled in a clean room environment and contains the disks and actuator assembly. Air is constantly circulated and filtered when the drive is operational. Venting of the HDA is accomplished via a breather filter.

The spindle is driven directly by an in-hub, brushless, sensorless DC drive motor. Dynamic braking is used to quickly stop the spindle.

3.3 Actuator

The read/write heads are mounted in the actuator. The actuator is a swing-arm assembly driven by a voice coil motor. A closed-loop positioning servo controls the movement of the actuator. An embedded servo pattern supplies feedback to the positioning servo to keep the read/write heads centered over the desired track.

The actuator assembly is balanced to allow vertical or horizontal mounting without adjustment.

When the drive is powered off, the actuator automatically moves the head to the actuator ramp outside of the disk where it parks.

4.0 Drive characteristics

4.1 Default logical drive parameters

Table 1: Formatted capacities

	HDS722540VLAT20	HDS722580VLAT20	HDS722512VLAT20 HDS722512VLAT80
Physical Layout			
Label capacity (GB)	40	80	120
Bytes per sector	512	512	512
Sectors per track	567-1170	567-1170	567-1170
Number of heads	1	2	3
Number of disks	1	1	2
Data sectors per cylinder	567-1170	1134-2340	1701-3510
Data cylinders per zone	1444-4501 (90KTPI) 1000-6846 (87KTPI)	1444-4501 (90KTPI) 1000-6846 (87KTPI)	1444-4501
Logical layout[1]			
Number of heads	16	16	16
Number of Sectors per track	63	63	63
Number of Cylinders[2]	16,383	16,383	16,383
Number of sectors	80,418,240	160,836,480	241,254,720
Total logical data bytes	41,174,138,880	82,348,277,760	123,522,416,640

	HDS722516VLAT20 HDS722516VLAT80	HDS722525VLAT80
Physical Layout		
Label capacity (GB)	160	250
Bytes per sector	512	512
Sectors per track	567-1170	567-1170
Number of heads	4	6
Number of disks	2	3
Data sectors per cylinder	2268-4680	3402-7020
Data cylinders per zone	1444-4501	1500-5000
Logical layout[1]		
Number of heads	16	16
Number of Sectors per track	63	63
Number of Cylinders[2]	16,383	16,383
Number of sectors	321,672,960	488,397,168
Total logical data bytes	164,696,555,520	250,059,350,016

Notes:

[1.] Number of cylinders: For drives with capacities greater than 8.45 GB the Identify Device information word 01 limits the number of cylinders to 16, 383 per the ATA specification.

[2.] Logical layout: Logical layout is an imaginary drive parameter (that is, the number of heads) which is used to access the drive from the system interface. The logical layout to Physical layout (that is, the actual Head and Sectors) translation is done automatically in the drive. The default setting can be obtained by issuing an IDENTIFY DEVICE command.

4.2 Data sheet

Table 2: Mechanical positioning performance

Data transfer rates (Mbps)	757
Interface transfer rates (Mb/s)	100
Data buffer size[1] (KB)	2048 / 8192
Rotational speed (RPM)	7200
Number of buffer segments (read)	up to 128
Number of buffer segments (write)	up to 63
Recording density - max (Kbpi)	689
Track density [TPI]	87/90 (40/80GB) 90 (120/160GB) 90/93.5 (250GB)
Areal density - max (Gbits/in^2)	62
Number of data bands	30

4.3 Drive organization

4.3.1 Drive format

Upon shipment from manufacturing the drive satisfies the sector continuity in the physical format by means of the defect flagging strategy described in Section 5.0, “Defect flagging strategy” on page 21 in order to provide the maximum performance to users.

4.3.2 Cylinder allocation

Table 3: Cylinder allocation

Zone	Physical cylinders			Blk/Trk
	87KTPI	90KTPI	93.5KTPI	
0	6,846	1,444	1,500	1,170
1	4,445	3,095	4,400	1,147
2	1,445	3,095	4,400	1,147
3	2,326	3,389	3,961	1,134
4	2,299	3,043	3,396	1,125
5	6,587	3,845	5,000	1,080
6	6,087	3,946	5,000	1,080
7	5,611	4,501	3,800	1,026
8	2,111	4,001	3,800	1,026
9	1,465	3,232	3,112	1,012
10	2,508	3,726	3,663	990
11	2,526	3,193	2,070	972
12	4,030	4,286	2,868	945
13	3,822	3,120	3,033	918
14	2,797	3,093	3,006	900
15	2,039	3,106	2,728	877
16	2,242	4,037	2,947	855
17	3,434	4,073	3,400	810
18	3,434	3,573	3,400	810
19	2,666	3,276	3,400	742
20	2,667	2,675	3,400	742
21	2,504	2,408	3,229	720
22	1,702	1,960	1,829	702
23	1,499	1,568	2,150	675
24	1,499	1,568	2,150	675
25	2,096	2,082	2,283	630

Table 3: Cylinder allocation

26	1,546	2,157	2,285	630
27	1,500	1,700	1,748	607
28	1,000	1,570	1,700	594
29	1,056	1,521	2,100	567

Physical cylinder is calculated from the starting data track of 0. It is not relevant to logical CHS. Depending on the capacity some of the inner zone cylinders are not allocated.

Data cylinder

This cylinder contains the user data which can be sent and retrieved via read/write commands and a spare area for reassigned data.

Spare cylinder

The spare cylinder is used by Hitachi Global Storage Technologies manufacturing and includes data sent from a defect location.

4.4 Performance characteristics

Drive performance is characterized by the following parameters:

- Command overhead
- Mechanical head positioning
  - Seek time
  - Latency
- Data transfer speed
- Buffering operation (Look ahead/Write cache)

All the above parameters contribute to drive performance. There are other parameters that contribute to the performance of the actual system. This specification tries to define the bare drive characteristics, not system throughput, which depends on the system and the application.

4.4.1 Command overhead

Command overhead is defined as the time required from the time the command is written into the command register by a host to the assertion of DRQ for the first data byte of a READ command when the requested data is not in the buffer excluding Physical seek time and Latency.

The table below gives average command overhead.

Table 4: Command overhead

Command type (Drive is in quiescent state)	Time (typical) (ms)	Time (typical) for queued command (ms)
Read (cache not hit) (from Command Write to Seek Start)	0.5	0.5
Read (cache hit) (from Command Write to DRQ)	0.1	0.1
Write (from Command Write to DRQ)	0.015	0.05
Seek (from Command Write to Seek Start)	0.5	not applicable

4.4.2 Mechanical positioning

4.4.2.1 Average seek time (including settling)

Table 5: Mechanical positioning performance

Command type		Typical (ms)	Max (ms)
Read	120-250GB	8.2	9.2
	40-80GB	8.5	9.5
Write	120-250GB	9.2	10.2
	40-80GB	9.5	10.5
Read (Quiet Seek mode)		19.5	20.5
Write (Quiet Seek mode)		20.5	21.5

The terms “Typical” and “Max” are used throughout this document and are defined as follows:

Typical The average of the drive population tested at nominal environmental and voltage conditions.

Max Maximum value measured on any one drive over the full range of the environmental and voltage conditions. (See Section 6.2, “Environment” on page 27 and Section 6.3, “DC power requirements” on page 29 for ranges.)

The seek time is measured from the start of the actuator’s motion to the start of a reliable read or write operation. A reliable read or write implies that error correction or recovery is not used to correct arrival problems. The average seek time is measured as the weighted average of all possible seek combinations.

$$\text{Weighted Average} = \frac{\sum_{n=1}^{max} (m10\ n)(Tnin + Tnout)}{(max + 1)(max)}$$

where

max = Maximum seek length
n = Seek length (1 to max)
Tnin = Inward measured seek time for an n track seek
Tnout = Outward measured seek time for an n track seek

4.4.2.2 Full stroke seek time (without command overhead, including settling)

Table 6: Full stroke seek time

Function		Typical (ms)	Max (ms)
Read	120-250GB	14.7	17.7
	40-80GB	15.1	18.1
Write	120-250GB	15.7	18.7
	40-80GB	16.1	19.1
Read (Quiet Seek mode)		32.5	35.5
Write (Quiet Seek mode)		33.5	36.5

Full stroke seek is measured as the average of 1,000 full stroke seeks with a random head switch from both directions (inward and outward).

4.4.2.3 Head switch time (head skew)

Table 7: Head switch time

	Head switch time-typical (ms)
87/90/93.5 KTPI	1.4

Head switch time is defined as the amount of time required by the fixed disk to complete a seek of the next sequential track after reading the last sector in the current track

The measuring method is given in 4.4.5, “Throughput” on page 19.

4.4.2.4 Cylinder switch time (cylinder skew)

Cylinder switch time is defined as the amount of time required by the fixed disk to access the next sequential block after reading the last sector in the current cylinder.

The measuring method is given in Section 4.4.5, “Throughput” on page 19.

4.4.2.5 Single track seek time (without command overhead, including settling)

Table 8: Single track seek time

Function	Typical (ms)	Max (ms)
Read	0.8	1.5
Write	1.3	2.0
Read (Quiet Seek mode)	0.8	1.5
Write (Quiet Seek mode)	1.3	2.0

Single track seek is measured as the average of one (1) single track seek from every track in both directions (inward and outward).

4.4.2.6 Average latency

Table 9: Latency Time

Rotational speed (RPM)	Time for one revolution (ms)	Average latency (ms)
7200 RPM	8.3	4.17

4.4.3 Drive ready time

Table 10: Drive ready time

Power on to ready	Typical (sec)	Maximum (sec)
80 GB models	6	31
160 GB models	8	31
250 GB models	10	31

Ready The condition in which the drive is able to perform a media access command (for example- read, write) immediately.

Power on This includes the time required for the internal self diagnostics.

Note: Max Power On to ready time is the maximum time period that Device 0 waits for Device 1 to assert PDIAG.

4.4.4 Data transfer speed

Table 11: Data transfer speed

Data transfer speed	250GB model (Mbytes/s)
Disk-Buffer transfer (Zone 0)	
Instantaneous - typical	72.1
Sustained - read typical	61.4
Disk-Buffer transfer (Zone 29)	
Instantaneous - typical	34.9
Sustained - read typical	29.7
Buffer - host (max)	100

- Instantaneous disk-buffer transfer rate (Mbyte/s) is derived by the following formula:

  ```
  512 (Number of sectors on a track) (revolutions per second)
  ```

  Note: The number of sectors per track will vary because of the linear density recording.

- Sustained disk-buffer transfer rate (Mbyte/s) is defined by considering head/cylinder change time for read operation. This gives a local average data transfer rate. It is derived by the following formula:

  ```
  (Sustained Transfer Rate) = A/(B+C+D)
  ```

  where

  ```
  A = 512 (number of data sectors per cylinder)
  B = (number of Surfaces per cylinder – 1) (head switch time)
  C = cylinder change time
  D = (number of surfaces) (time for one revolution)
  ```

- Instantaneous buffer-host transfer rate (Mbyte/s) defines the maximum data transfer rate on the AT Bus. It also depends on the speed of the host.

The method of measurement is given in 4.4.5, “Throughput” on page 19.

4.4.5 Throughput

4.4.5.1 Simple sequential access

The following table illustrates simple sequential access for the three-disk enclosure.

Table 12: Simple Sequential Access performance

Operation	Typical (sec)	Max (sec)
Sequential Read (Zone 0)	0.3	0.32
Sequential Read (Zone 29)	0.61	0.64

The above table gives the time required to read a total of 8000h consecutive blocks (16,777,216 bytes) accessed by 128 read commands. Typical and Max values are given by 105% and 110% of T respectively throughout following performance description.

```
T = A + B + C + 16,777,216/D + 512/E  (READ)
```

where

```
T = Calculated time (sec)
A = Command process time (Command overhead) (sec)
B = Average seek time (sec)
C = Average latency (sec)
D = Sustained disk-buffer transfer rate (byte/sec)
E = Buffer-host transfer rate (byte/sec)
```

Note: It is assumed that a host system responds instantaneously and host data transfer is faster than sustained data rate.

4.4.5.2 Random access

The following table illustrates simple sequential access for three-disk enclosure.

Table 13: Random Access performance

Table 14: Random Access Performance

Operation	Typical (sec)	Max (sec)
Random Read	55.5	58.1

The above table gives the time required to execute a total of 1000h read commands which access a single random LBA. Typical and Max values are given by 105% and 110% of T respectively throughout following performance description.

```
T = 4096(A + B + C+ 512/D + 512/E)  (READ)
```

where

```
T = Calculated time (sec)
A = Command process time (Command overhead) (sec)
```

```
B = Average seek time (sec)
C = Latency
D = Average sustained disk-buffer transfer rate (byte/s)
E = Buffer-host transfer rate (byte/s)
```

4.4.6 Operating modes

4.4.6.1 Description of operating modes

Table 15: Description of operating modes

Operating mode	Description
Spin-up	Start up time period from spindle stop or power down.
Seek	Seek operation mode
Write	Write operation mode
Read	Read operation mode
Unload Idle	Spindle rotation at 7200 RPM with heads unloaded.
Idle	Spindle motor and servo system are working normally. Commands can be received and processed immediately.
Standby	Actuator is unloaded and spindle motor is stopped. Commands can be received immediately.
Sleep	TActuator is unloaded and spindle motor is stopped. Only soft reset or hard reset can change the mode to standby.

Note: Upon power down or spindle stop a head locking mechanism will secure the heads in the OD parking position.

4.4.6.2 Mode transition time

Table 16: Mode transition time

From	To	RPM	Transition time (sec)	
			Typical	Maximum
Standby	Idle	0 ---> 7200 (3disks)	9	31
Idle	Standby	7200 ---> 0	Immediately	Immediately
Standby	Sleep	0	Immediately	Immediately
Sleep	Standby	0	Immediately	Immediately
Unload idle	Idle	7200	0.7	
Idle	Unload idle	7200	0.7	

"Immediately" means within 1ms.

Note: The command is processed immediately but there will be an actual spin down time reflecting the seconds passed until the spindle motor stops.

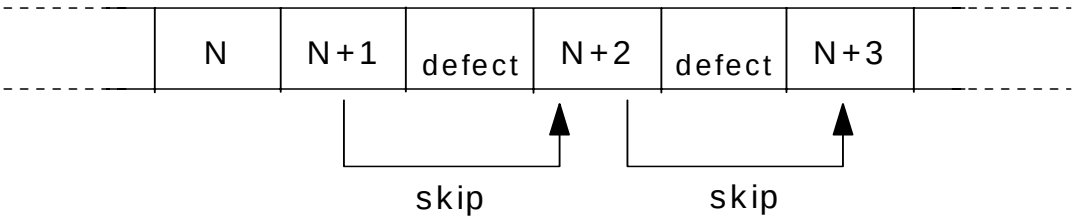
5.0 Defect flagging strategy

Media defects are remapped to the next available sector during the Format Process in manufacturing. The mapping from LBA to the physical locations is calculated by an internally maintained table.

Shipped format

- Data areas are optimally used.
- No extra sector is wasted as a spare throughout user data areas.
- All pushes generated by defects are absorbed by the spare tracks of the inner zone.

Table 17: Plist physical format



Defects are skipped without any constraint, such as track or cylinder boundary.

6.0 Specification

6.1 Jumper settings

6.1.1 Jumper pin location

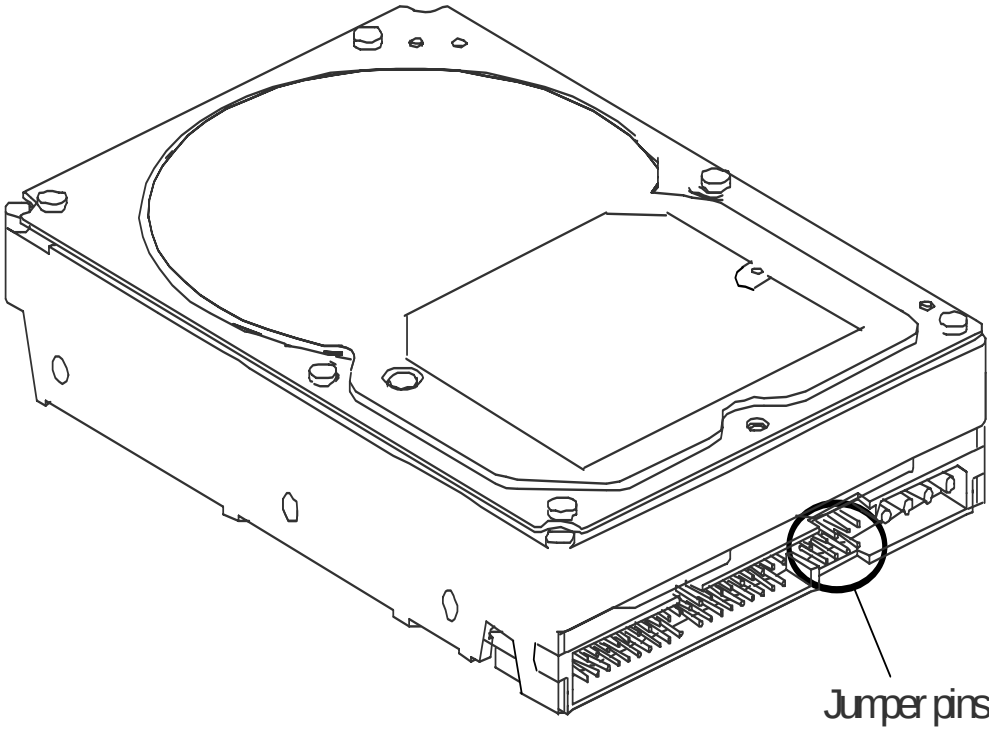


Figure 1: Jumper pin location

6.1.2 Jumper pin identification

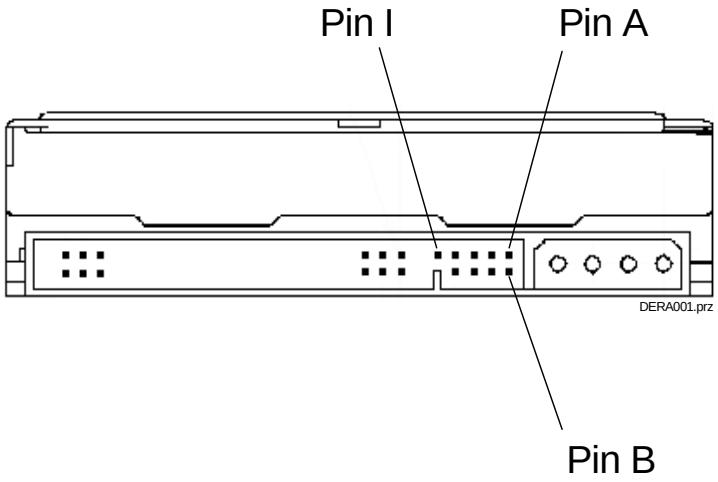


Figure 2: Jumper pin identification

6.1.3 Jumper pin assignment

There are four jumper settings as shown in the following sections:

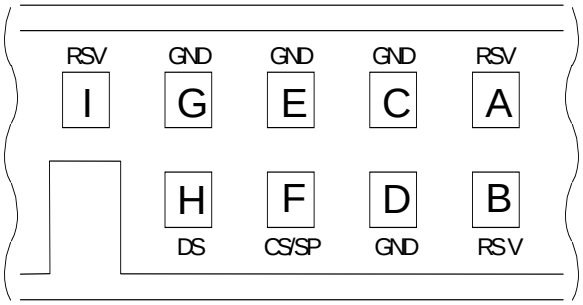
- 16 logical head default (normal use)
- 15logical head default
- 32 GB clip
- Power up in standby

Within each of these four jumper settings the pin assignment selects Device 0, Device 1, Cable Selection, or Device 1 Slave Present as shown in the following figures.

The Device 0 setting automatically recognizes device 1 if it is present.

The Device 1 Slave Present setting is for a slave device that does not comply with the ATA specification.

Note: In conventional terminology "Device 0" designates a Master and "Device 1" designates a Slave.



6.1.4 Jumper positions

6.1.4.1 16 logical head default (normal use)

The figure below shows the jumper positions used to select Device 0, Device 1, Cable Selection, or Device1 (Slave) Present.

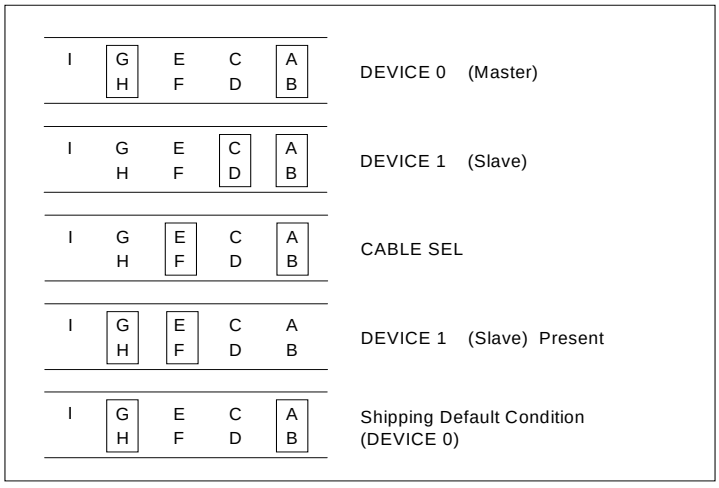


Figure 3: Jumper positions for normal use

Notes:

1. To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In the CSEL mode the drive address is determined by AT interface signal #28 CSEL as follows:
   - When CSEL is grounded or at a low level, the drive address is 0 (Device 0).
   - When CSEL is open or at a high level, the drive address is 1 (Device 1).
2. In CSEL mode, installing or removing the jumper blocks at A-B or C-D position does not affect any selection of Device or Cable Selection mode.
3. The shipping default position is the Device 0 position.

6.1.4.2 15 logical head default

The figure below shows the jumper positions used to select Device 0, Device 1, Cable Selection, or Device1 (Slave) Present setting 15 logical heads instead of default 16 logical head models.

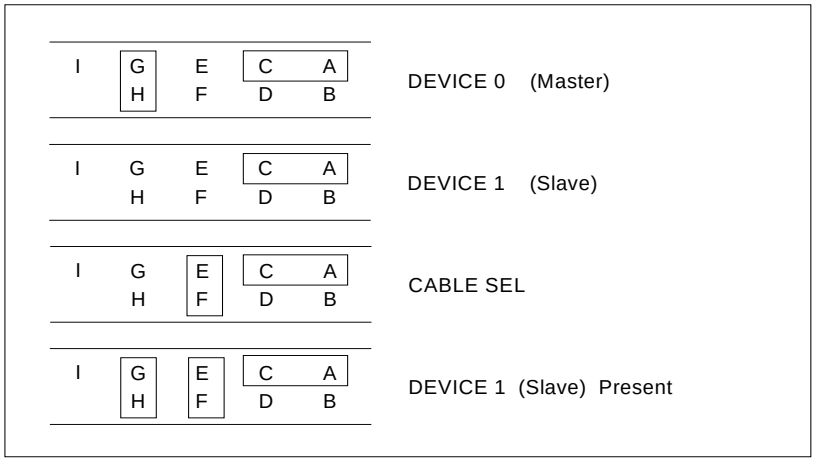


Figure 4: Jumper positions for 15 head logical default

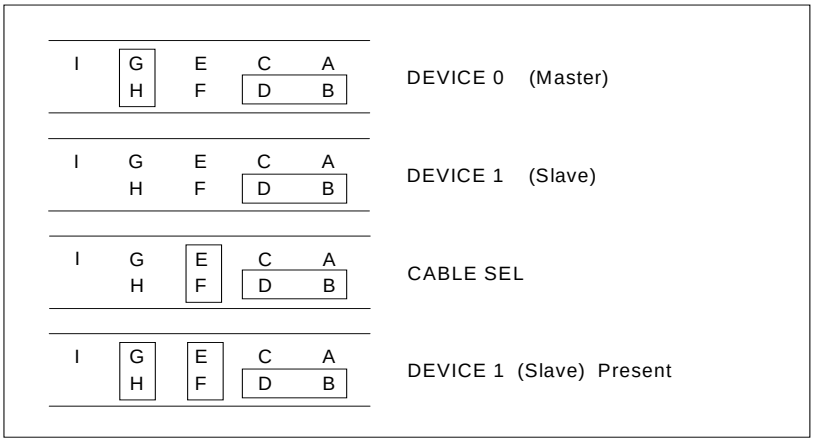
Notes:

1. To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In the CSEL mode the drive address is determined by AT interface signal #28 CSEL as follows:
   - When CSEL is grounded or at a low level, the drive address is 0 (Device 0).
   - When CSEL is open or at a high level, the drive address is 1 (Device 1).
2. In CSEL mode, installing or removing the jumper blocks at A-B or C-D position does not affect any selection of Device or Cable Selection mode.

6.1.4.3 Capacity clip to 32GB

The figure below shows the jumper positions used to select Device 0, Device 1, Cable Selection, or Device1 (Slave) Present while setting the drive capacity down to 32 GB for the purpose of compatibility.

Table 18: Jumper positions for capacity clip to 32GB

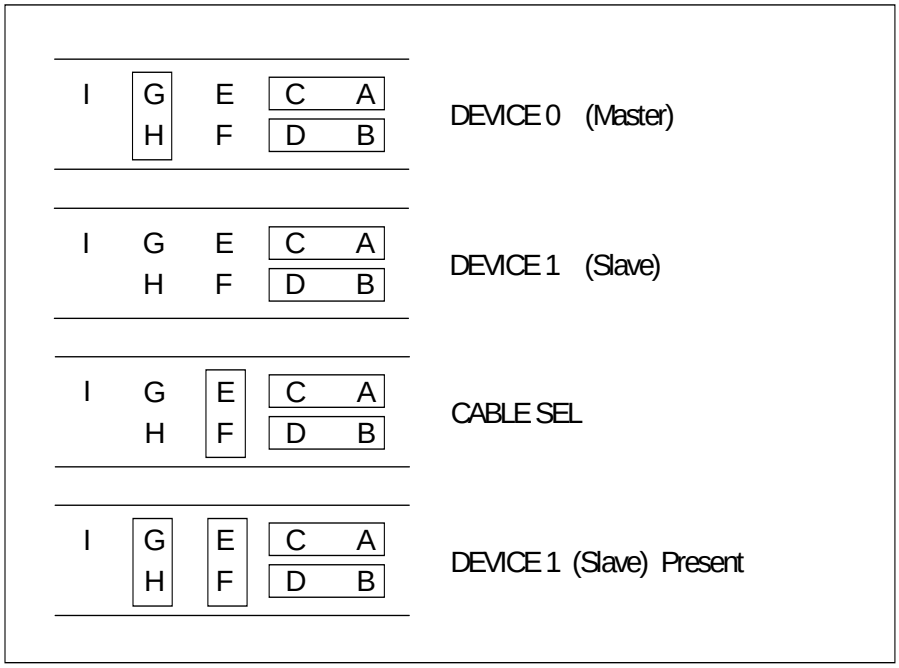


Note: The jumper setting acts as a 32GB clip which clips the LBA to 66055248. The CHS is unchanged from the factory default of 16383/16/63.

6.1.4.4 Power up in Standby

The figure below shows the jumper positions used to select Device 0, Device 1, Cable Selection, or Device1 (Slave) Present to enable Power Up In Standby.

Table 19: Jumper settings for Disabling Auto Spin



Notes:

1. These jumper settings are used for limiting power supply current when multiple drives are used.
2. Command to spin up is SET FEATURES (subcommand 07h). Refer to 12.28 Set Features.
3. To enable the CSEL mode (Cable Selection mode) the jumper block must be installed at E-F. In the CSEL mode the drive address is determined by AT interface signal #28 CSEL as follows:
   - When CSEL is grounded or at a low level, the drive address is 0 (Device 0).
   - When CSEL is open or at a high level, the drive address is 1 (Device 1).

6.2 Environment

6.2.1 Temperature and humidity

Table 20: Temperature and humidity

Operating conditions	
Temperature	5C to 55ºC (See note below)
Relative humidity	8 to 90%, non-condensing
Maximum wet bulb temperature	29.4ºC, non-condensing
Maximum temperature gradient	15ºC/hour
Altitude	–300 to 3,048 m
Non-operating conditions	
Temperature	–40C to 65ºC
Relative humidity	5 to 95%, non-condensing
Maximum wet bulb temperature	35ºC, non-condensing
Altitude	–300 to 12,000 m

Notes:

- The system is responsible for providing sufficient ventilation to maintain a surface temperature below 60°C at the center of the top cover of the drive.
- Noncondensing conditions should be maintained at any time.
- Maximum storage period within shipping package is one year.

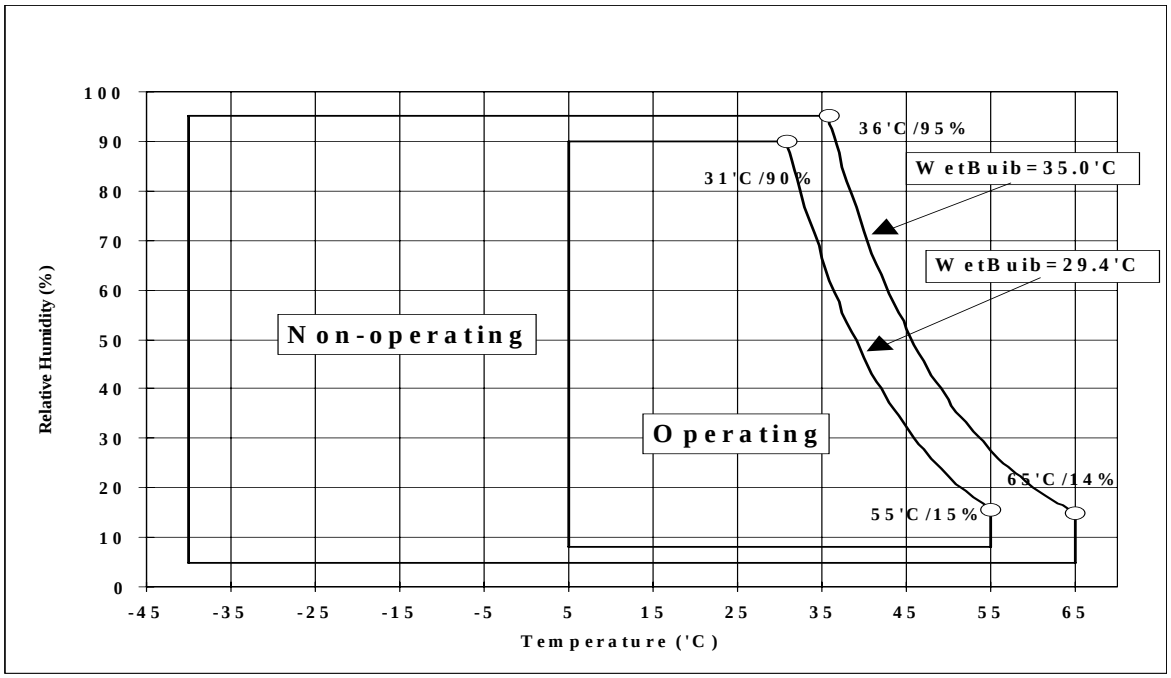


Figure 5: Limits of temperature and humidity

6.2.2 Corrosion test

The drive shows no sign of corrosion inside and outside of the hard disk assembly and is functional after being subjected to seven days at 50°C with 90% relative humidity.

6.3 DC power requirements

Damage to the drive electronics may result if the power supple cable is connected or disconnected to the legacy power connector while power is being applied to the drive (no hot plug/unplug is alloweed). If SATA power supply cable is connected or disconnected to the SATA power connector, hot plug/unplug is allowed.

6.3.1 Input voltage

Table 21: Input voltage

Input voltage supply	During run and spin up	Absolute max spike voltage[1]
+5 V	5 V ± 5%	–0.3 to 7 V
+12 V	12 V + 10% –8%	–0.3 to 15 V

[1]*To avoid damage to the drive electronics, power supply voltage spikes must not exceed specifications.*

6.3.2 Power supply current (typical)

Table 22: Power supply current of xxx-GB models

Power supply current of 250-GB model values in milliamps, RMS	**+5 Volts (mA)**		**+12 Volts (mA)**		**Total (W)**
	Pop mean	Std dev	Pop mean	Std dev	
Idle average	280	12	470	12	7.0
Idle ripple (peak-to-peak)	230	40	330	20	
Low RPM idle	140	7	180	10	2.9
Low RPM idle ripple	220	25	270	20	
Unload idle average	140	7	350	13	4.9
Unload idle ripple	220	25	240	20	
Random R/W average	430	9	660	14	10.1
Random R/W peak	1252	50	1750	50	
Silent R/W average[2]	470	9	470	15	8.0
Silent R/W peak	1252	50	995	40	
Start up (max)	870	51	1840	75	
Standby average	140	9	20	3	0.9
Sleep average	100	8	20	3	0.7

Except for a peak of less than 100 ms duration

[1] Random seeks at 40% duty cycle

[2] Seek duty = 30%, W/R duty = 45%, Idle duty = 25%

Power supply current of 120 GB and 160 GB models values in milliamps, RMS	**+5 Volts (mA)**		**+12 Volts (mA)**		**Total (W)**
	Pop mean	Std dev	Pop mean	Std dev	
Idle average	280	12	375	12	5.9
Idle ripple (peak-to-peak)	230	40	250	20	
Low RPM idle	140	7	140	10	2.4
Low RPM idle ripple	220	25	170	20	
Unload idle average	140	7	300	13	4.3
Unload idle ripple	220	25	220	20	
Random R/W average	430	9	590	12	9.2
Random R/W peak	1252	30	1600	50	
Silent R/W average[2]	470	9	390	12	7.0
Silent R/W peak	1252	50	890	40	
Start up (max)	870	50	1750	50	
Standby average	140	9	20	3	0.9
Sleep average	100	8	20	3	0.7

Power supply current of 40GB and 80GB models values in milliamps, RMS	**+5 Volts (mA)**		**+12 Volts (mA)**		**Total (W)**
	Pop mean	Std dev	Pop mean	Std dev	
Idle average	280	12	300	12	5.0
Idle ripple (peak-to-peak)	230	40	220	20	
Low RPM idle	140	7	130	10	2.3
Low RPM idle ripple	220	25	160	20	
Unload idle average	140	7	270	12	3.9
Unload idle ripple	220	25	200	20	
Random R/W average	430	9	590	12	9.2
Random R/W peak	1252	50	1720	65	
Silent R/W average[2]	470	9	370	12	6.8
Silent R/W peak	1252	50	830	40	

Power supply current of 40GB and 80GB models values in milliamps, RMS	+5 Volts (mA)		+12 Volts (mA)		Total (W)
	Pop mean	Std dev	Pop mean	Std dev	
Start up (max)	870	50	1700	50	
Standby average	140	9	20	3	0.9
Sleep average	100	8	20	3	0.7

6.3.3 Power supply generated ripple at drive power connector

Table 23: Power supply generated ripple at drive power connector

	Maximum (mV pp)	MHz
+5 V dc	100	0-10
+12 V dc	150	0-10

During drive start up and seeking 12-volt ripple is generated by the drive (referred to as dynamic loading). If the power of several drives is daisy chained together, the power supply ripple plus the dynamic loading of the other drives must remain within the above regulation tolerance. A common supply with separate power leads to each drive is a more desirable method of power distribution.

To prevent external electrical noise from interfering with the performance of the drive, the drive must be held by four screws in a user system frame which has no electrical level difference at the four screws position and has less than ±300 millivolts peak to peak level difference to the ground of the drive power connector.

6.4 Reliability

6.4.1 Data integrity

No more than one sector is lost at Power loss condition during the write operation when the write cache option is disabled. If the write cache option is active, the data in write cache will be lost. To prevent the loss of customer data, it is recommended that the last write access before power off be issued after setting the write cache off.

6.4.2 Cable noise interference

To avoid any degradation of performance throughput or error rate when the interface cable is routed on top or comes in contact with the HDA assembly, the drive must be grounded electrically to the system frame by four screws. The common mode noise or voltage level difference between the system frame and power cable ground or AT interface cable ground should be in the allowable level specified in the power requirement section.

6.4.3 Start/stop cycles

The drive withstands a minimum of 50,000 start/stop cycles in a 40° C environment and a minimum of 10,000 start/stop cycles in extreme temperature or humidity within the operating range. See Table 20: “Temperature and humidity” on page 28 and Figure 5: “Limits of temperature and humidity” on page 28.

6.4.4 Preventive maintenance

None

6.4.5 Data reliability

Probability of not recovering data is 1 in 10^{14} bits read

ECC On The Fly correction

- 1 Symbol : 8 bits
- 4 Interleave
- 12 ECCs are embedded into each interleave
- This implementation always recovers 5 random burst errors and a 153-bit continuous burst error

6.4.6 Required power-off sequence

The required BIOS sequence for removing power from the drive is as follows:

Step 1: Issue one of the following commands.

Standby
Standby immediate
Sleep

Note: Do not use the Flush Cache command for the power off sequence because this command does not invoke Unload

Step 2: Wait until the Command Complete status is returned. In a typical case 350 ms are required for the command to finish completion; however, the BIOS time out value needs to be 30 seconds considering error recovery time. Refer to section13.0 “Time-out values” on page 221.

Step 3: Terminate power to HDD.

6.5 Mechanical specifications

6.5.1 Physical dimensions and weight

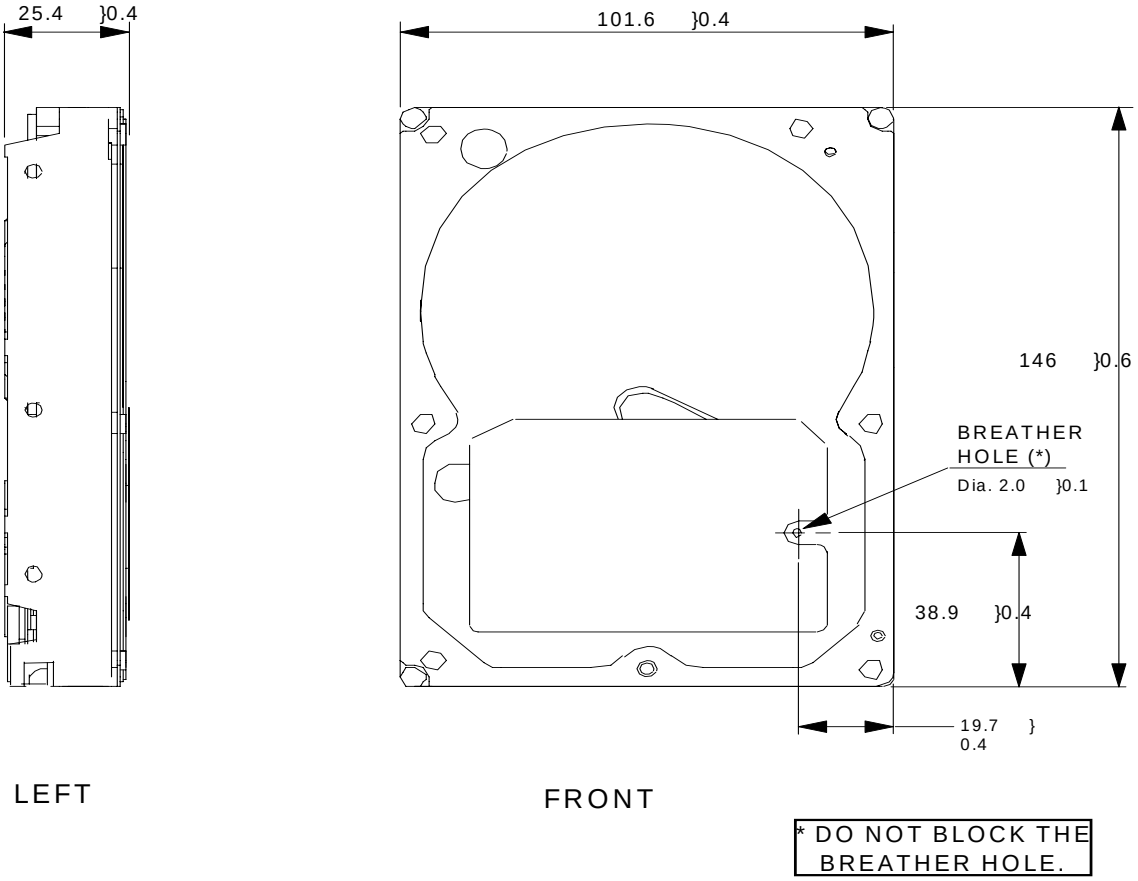


Figure 6: Top and side view of 120GB - 250GB models with mechanical dimensions

All dimensions in the above figure are in millimeters.

The breather hole must be kept uncovered in order to keep the air pressure inside of the disk enclosure equal to external air pressure.

The following table lists the dimensions of the drive.

Table 24: Physical dimensions and weight

Height [mm]	25.4±0.4
Width [mm]	101.6±0.4
Length [mm]	146.0±0.6
Weight [grams - maximum]	640

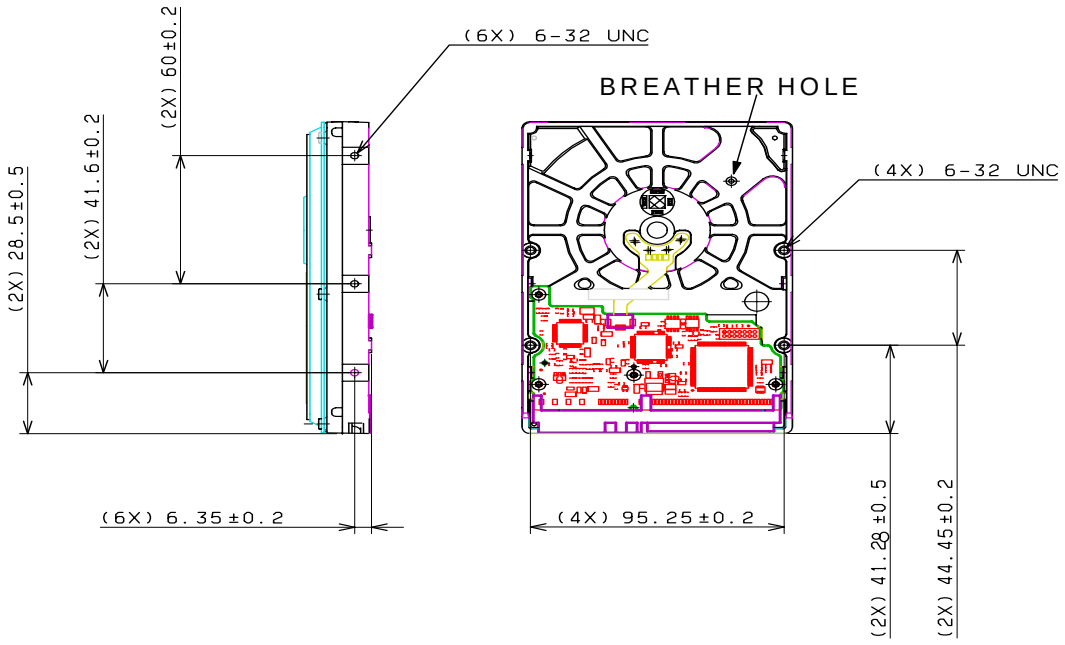


Figure 7: Bottom and side of 40GB - 80GB view with breather hole and mounting hole locations

6.5.2 Mounting hole locations

The mounting hole locations and size of the drive are shown below. All dimensions are in mm.

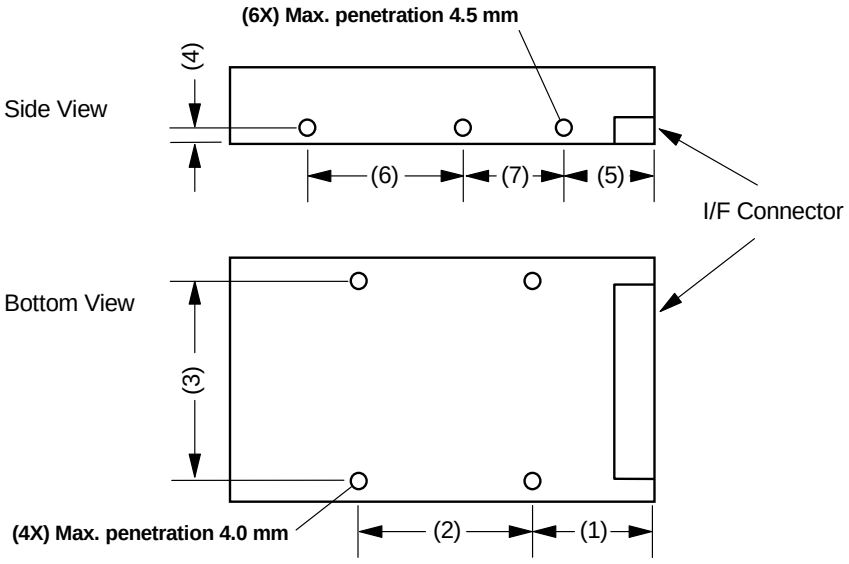


Figure 8: Mounting hole locations

Thread	(1)	(2)	(3)	(4)	(5)	(6)	(7)
6-32 UNC	41.28±0.5	44.45±0.2	95.25±0.2	6.35±0.2	28.5±0.5	60.0±0.2	41.6±0.2

6.5.3 Connector locations

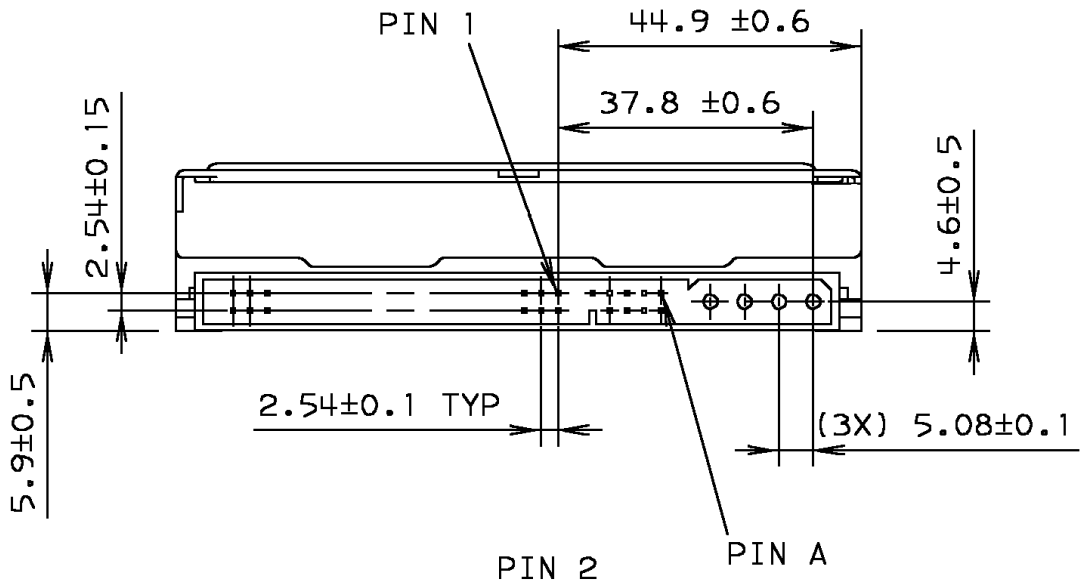


Figure 9: Connector locations

6.5.4 Drive mounting

The drive will operate in all axes (6 directions). Performance and error rate will stay within specification limits if the drive is operated in the other orientations from which it was formatted.

For reliable operation, the drive must be mounted in the system securely enough to prevent excessive motion or vibration of the drive during seek operation or spindle rotation, using appropriate screws or equivalent mounting hardware.

The recommended mounting screw torque is 0.6 - 1.0 Nm (6-10 Kgf.cm).

The recommended mounting screw depth is 4 mm maximum for bottom and 4.5 mm maximum for horizontal mounting.

Drive level vibration test and shock test are to be conducted with the drive mounted to the table using the bottom four screws.

6.5.5 Heads unload and actuator lock

The head load/unload mechanism is provided to protect the disk data during shipping, movement, or storage. Upon power down, the heads are automatically unload from the disk area and the locking mechanism of the head actuator will secure the heads in unload position.

6.6 Vibration and shock

All vibration and shock measurements recorded in this section are made with a drive that has no mounting attachments for the systems. The input power for the measurements is applied to the normal drive mounting points.

6.6.1 Operating vibration

6.6.1.1 Random vibration

The test is 30 minutes of random vibration using the power spectral density (PSD) levels shown below in each of three mutually perpendicular axes. The disk drive will operate without non-recoverable errors when subjected to the above random vibration levels.

The overall RMS (root mean square) level is 0.67 G for horizontal vibration and 0.56 G for vertical.

Table 25: Random vibration PSD

Table 26: Random vibration PSD profile break points (operating)

Direction	5Hz	17Hz	45Hz	48Hz	62Hz	65Hz	150Hz	200Hz	500Hz	RMS (G)
Horizontal x10–3 [G2/Hz	0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.5	0.5	0.67
Vertical x10–3 [G2/Hz]	0.02	1.1	1.1	8.0	8.0	1.0	1.0	0.08	0.08	0.56

The overall RMS (root mean square) level is 0.67 G for horizontal vibration and 0.56 G for vertical.

6.6.1.2 Swept sine vibration

The drive will meet the criteria shown below while operating in the specified conditions:

- No errors occur with 0.5 G 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3-minute dwells at two major resonances
- No data loss occurs with 1 G 0 to peak, 5 to 300 to 5 Hz sine wave, 0.5 oct/min sweep rate with 3-minute dwells at two major resonances

6.6.2 Nonoperating vibration

The drive does not sustain permanent damage or loss of previously recorded data after being subjected to the environment described below

6.6.2.1 Random vibration

The test consists of a random vibration applied in each of three mutually perpendicular axes for a duration of 10 minutes per axis. The PSD levels for the test simulate the shipping and relocation environment shown below.

Table 27: Random Vibration PSD profile breakpoints (nonoperating)

Frequency	2Hz	4Hz	8Hz	40Hz	55Hz	70Hz	200Hz
G2/Hz	0.001	0.03	0.03	0.003	0.01	0.01	0.001

The overall RMS (root mean square) level of vibration is 1.04 G.

6.6.2.2 Swept sine vibration

- 2 G (zero-to-peak), 5 to 500 to 5 Hz sine wave
- 0.5 oct/min sweep rate
- 3 minutes dwell at two major resonances

6.6.3 Operating shock

The drive meets the following criteria while operating in the conditions described below. The shock test consists of 10 shock inputs in each axis and direction for total of 60. There must be a delay between shock pulses long enough to allow the drive to complete all necessary error recovery procedures.

- No error occurs with a 10 G half-sine shock pulse of 11 ms duration in all models.
- No data loss occurs with a 30 G half-sine shock pulse of 4 ms duration in all models.
- No data loss occurs with a 55 G half-sine shock pulse of 2 ms duration in all models.

6.6.4 Nonoperating shock

The drive will operate with no degradation of performance after being subjected to shock pulses with the following characteristics.Trapezoidal shock wave

6.6.4.1 Trapezoidal shock wave

- Approximate square (trapezoidal) pulse shape
- Approximate rise and fall time of pulse is 1 ms
- Average acceleration level is 50 G. (Average response curve value during the time following the 1 ms rise time and before the 1 ms fall with a time "duration of 11 ms")
- Minimum velocity change is 4.23 meters per second

6.6.4.2 Sinusoidal shock wave

The shape is approximately half-sine pulse. The figure below shows the maximum acceleration level and duration.

Table 28: Sinusoidal shock wave

Models	Acceleration level (G)	Duration (ms)
1 and 2 disk models	350	2
3 disk models	300	
All models	75	11

6.6.5 Nonoperating rotational shock

All shock inputs shall be applied around the actuator pivot axis.

Table 29: Rotational shock

Duration	Rad/s^2
1 ms	30,000
2 ms	20,000

6.7 Acoustics

The upper limit criteria of the octave sound power levels are given in Bels relative to one picowatt and are shown in the following table. The sound power emission levels are measured in accordance with ISO7779.

Table 30: Sound power levels

Mode		Typical/Max		
		1 disk model	2 disk model	3 disk model
Idle		2.6 / 3.0	2.8 / 3.2	3.0 / 3.4
Operating	Performance seek mode	3.4 / 3.7	3.4 / 3.7	3.4 / 3.7
	Quiet seek	2.8 / 3.2	2.9 / 3.3	3.1 / 3.5

Table 31: Sound power levels

Mode definitions

- I**dle mode:** The drive is powered on, disks spinning, track following, unit is ready to receive and respond to control line commands.
- **Operating mode:** Continuous random cylinder selection and seek operation of the actuator with a dwell time at each cylinder. The seek rate for the drive is calculated with the following formula:
    - Dwell time = 0.5 x 60/RPM
    - Seek rate = 0.4 / (average seek time + dwell time)

6.8 Identification labels

The following labels are affixed to every drive:

- A label containing the Hitachi logo, the Hitachi Global Storage Technologies part number and the statement " Made by Hitachi Global Storage Technologies Inc." or Hitachi Global Storage Technologies approved equivalent.
- A label containing the drive model number, the manufacturing date code, the formatted capacity, the place of manufacture, UL/CSA/TUV/CE/C-Tick mark logos
- A bar code label containing the drive serial number
- A label containing jumper pin description
- A user designed label per agreement

The above labels may be integrated with other labels

6.9 Safety

6.9.1 UL and CSA approval

The product is qualified per UL (Underwriters Laboratory) 1950 Third Edition and CAN/CSA C22.2 No.950-M95 Third Edition, for use in Information Technology Equipment, including Electric Business Equipment. The UL Recognition or the CSA certification is maintained for the product life. The UL and C-UL recognition mark or the CSA monogram for CSA certification appears on the drive.

6.9.2 German safety mark

All models are approved by TUV on Test Requirement: EN60950:1992+A1-4, but the GS mark is not applicable to internal devices such as this product.

6.9.3 Flammability

The printed circuit boards used in this drive are made of material with a UL recognized flammability rating of V-1 or better. The flammability rating is marked or etched on the board. All other parts not considered electrical components are made of material with a UL recognized flammability rating of V-1 or better. However, small mechanical parts such as cable ties, washers, screws, and PC board mounts may be made of material with a UL recognized flammability rating of V-2.

6.9.4 Safe handling

The product is conditioned for safe handling in regards to sharp edges and corners.

6.9.5 Environment

The product does not contain any known or suspected carcinogens.

Environmental controls meet or exceed all applicable government regulations in the country of origin. Safe chemical usage and manufacturing control are used to protect the environment. An environmental impact assessment has been done on the manufacturing process used to build the drive, the drive itself and the disposal of the drive at the end of its life.

Production also meets the requirements of the international treaty on chlorofluorocarbon (CFC) control known as the United Nations Environment Program Montreal Protocol, and as ratified by the member nations. Material to be controlled include CFC-11, CFC-12, CFC-113, CFC-114, CFC-115, Halon 1211, Halon 1301 and Halon 2402. Although not specified by the Protocol, CFC-112 is also controlled. In addition to the Protocol Hitachi Global Storage Technologies requires the following:

- that no packaging used for the shipment of the product use controlled CFCs in the manufacturing process.
- that no manufacturing processes for parts or assemblies include printed circuit boards use controlled CFC materials.

6.9.6 Secondary circuit protection

Spindle/VCM driver module includes 12 V over current protection circuit

6.10 Electromagnetic compatibility

The drive, when installed in a suitable enclosure and exercised with a random accessing routine at maximum data rate meets the worldwide EMC requirements listed below:

- United States Federal Communications Commission (FCC) Rules and Regulations (Class B), Part 15. (A 6 dB buffer shall be maintained on the emission requirements).
- European Economic Community (EEC) directive number 76/889 related to the control of radio frequency interference and the Verband Deutscher Elektrotechniker (VDE) requirements of Germany (GOP). IBM National Bulletin NB 2-0001-400, NB 2-0001-401, and NB 2-0001-403.

6.10.1 CE mark

The product is declared to be in conformity with requirements of the following EC directives under the sole responsibility of Hitachi Global Storage Technologies Japan Ltd:

Council Directive 89/336/EEC on the approximation of laws of the Member States relating to electromagnetic compatibility.

6.10.2 C-TICK mark

The product complies with the following Australian EMC standard:

Limits and methods of measurement of radio disturbance characteristics of information technology, AS/NZS 3548 :1995 Class B.

6.10.3 BSMI mark

The product complies with the Taiwan EMC standard"Limits and methods of measurement of radio disturbance characteristics of information technology equipment, CNS 13438 Class B."

6.11 Packaging

Drives are packed in ESD protective bags and shipped in appropriate containers.

7.0 Electrical interface specification

7.1 Connector location

Refer to the following illustration to see the location of the connectors

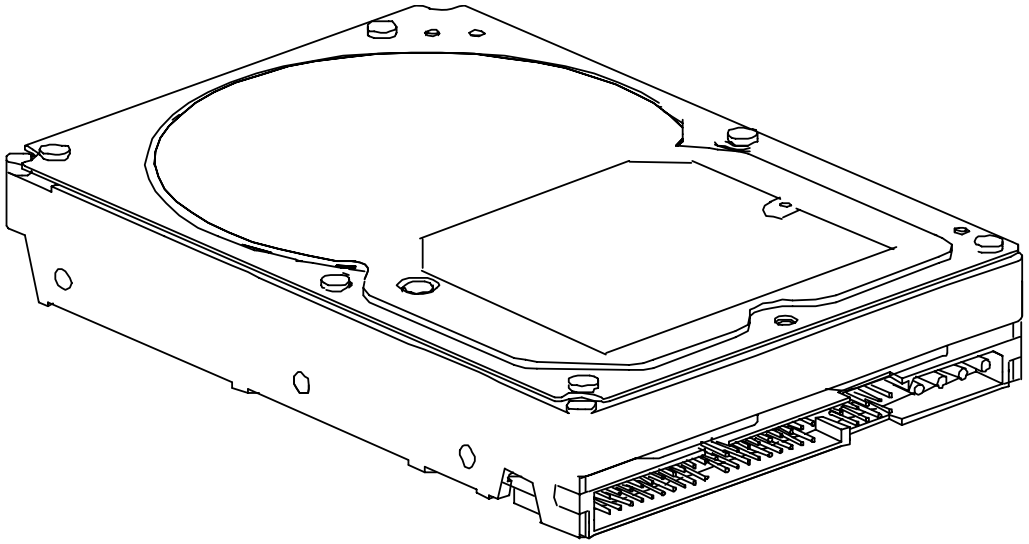
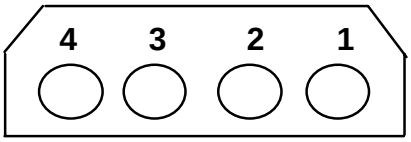


Figure 10 : Connector location

7.1.1 DC power connector

The DC power connector is designed to mate with AMP part number 1-480424-0 using AMP pins part number 350078-4 (strip), part number 61173-4 (loose piece), or their equivalents. Pin assignments are shown in the figure below.



Pin	Voltage
1	+12 V
2	GND
3	GND
4	+5V

Figure 11 : Power connector pin assignments

7.1.2 AT signal connector

The AT signal connector is a 40-pin connector.

7.2 Signal definitions

The pin assignments of interface signals are listed as follows:

Table 32: Signal definitions

PIN	SIGNAL	I/O	Type		PIN	SIGNAL	I/O	Type
01	RESET-	I	TTL		02	GND		
03	DD7	I/O	3–state		04	DD08	I/O	3–state
05	DD6	I/O	3–state		06	DD09	I/O	3–state
07	DD5	I/O	3–state		08	DD10	I/O	3–state
09	DD4	I/O	3–state		10	DD11	I/O	3–state
11	DD3	I/O	3–state		12	DD12	I/O	3–state
13	DD2	I/O	3–state		14	DD13	I/O	3–state
15	DD1	I/O	3–state		16	DD14	I/O	3–state
17	DD0	I/O	3–state		18	DD15	I/O	3–state
19	GND				(20)	Key		
21	DMARQ	O	3–state		22	GND		
23	DIOW-(*)	I	TTL		24	GND		
25	DIOR-(*)	I	TTL		26	GND		
27	IORDY-(*)	O	3–state		28	CSEL	I	TTL
29	DMACK-	I	TTL		30	GND		
31	INTRQ	O	3–state		32			
33	DA1	I	TTL		34	PDIAG-	I/O	OD
35	DA0	I	TTL		36	DA02	I	TTL
37	CS0-	I	TTL		38	CS1-	I	TTL
39	DASP-	I/O	OD		40	GND		

Notes:

O	designates an output from the drive
I	designates an input to the drive
I/O	designates an input/output common
OD	designates an Open-Drain output

The signal lines marked with (*) are redefined during the Ultra DMA protocol to provide special functions. These lines change from the conventional to special definitions at the moment the host decides to allow a DMA burst, if the Ultra DMA transfer mode was previously chosen via Set Features. The drive becomes aware of this change upon assertion of the DMACK- line. These lines revert back to their original definitions upon the deassertion of DMACK- at the termination of the DMA burst.

7.3 Signal descriptions

Table 33: Special signal definitions for Ultra DMA

	Special Definition (for Ultra DMA)	Conventional Definition
Write Operation	DDMARDY-	IORDY
	HSTROBE	DIOR-
	STOP	DIOW-
Read Operation	HDMARDY-	DIOR-
	DSTROBE	IORDY
	STOP	DIOW-

DD00–DD15

A 16-bit bi-directional data bus between the host and the drive. The lower 8 lines, DD00-07, are used for Register and ECC access. All 16 lines, DD00–15, are used for data transfer. These are 3-state lines with 24 mA current sink capability.

DA00–DA02

These are addresses used to select the individual register in the drive.

CS0-

The chip select signal generated from the Host address bus. When active, one of the Command Block Registers [Data, Error (Features when written), Sector Count, Sector Number, Cylinder Low, Cylinder High, Drive/Head and Status (Command when written) register] can be selected. (See Table 34: “I/O address map” on page 60.)

CS1-

The chip select signal generated from the Host address bus. When active, one of the Control Block Registers [Alternate Status (Device Control when written) and Drive Address register] can be selected. (See Table 34: “I/O address map” on page 60.)

RESET-

This line is used to reset the drive. It shall be kept at a Low logic state during power up and kept High thereafter.

DIOW-

The rising edge of this signal holds data from the data bus to a register or data register of the drive.

DIOR-

When this signal is low, it enables data from a register or data register of the drive onto the data bus. The data on the bus shall be latched on the rising edge of DIOR-

INTRQ

The interrupt is enabled only when the drive is selected and the host activates the IEN- bit in the Device Control Register. Otherwise, this signal is in high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. The IRQ is reset to zero by a host read of the status register or a write to the Command Register. This signal is a 3-state line with 24mA of sink capability.

DASP-

This is a time-multiplexed signal which indicates that a drive is active or that device 1 is present. This signal is driven by an Open-Drain driver and internally pulled up to 5 volts through a 10 kW resistor. During a Power-On initialization or after RESET- is negated, DASP- shall be asserted by Device 1 within 400 ms to indicate that device 1 is present. Device 0 shall allow up to 450 ms for device 1 to assert DASP-. If device 1 is not present, device 0 may assert DASP- to drive an LED indicator. The DASP- signal shall be negated following acceptance of the first valid command by device 1. Anytime after negation of DASP-, either drive may assert DASP- to indicate that a drive is active.

During Power-On initialization or after RESET- is negated, DASP- shall be asserted by Device 1 within 400 ms to indicate that device 1 is present. Device 0 shall allow up to 450ms for device 1 to assert DASP-. If device 1 is not present, device 0 may assert DASP- to drive a LED indicator.

DASP- shall be negated following acceptance of the first valid command by device 1. At anytime after negation of DASP-, either drive may assert DASP- to indicate that a drive is active.

PDIAG-

This signal shall be asserted by device 1 to indicate to device 0 that it has completed the diagnostics. This line is pulled up to 5 volts in the drive through a 10 kΩ resistor.

Following a Power On Reset, software reset, or RESET-, drive 1 shall negate PDIAG- within 1 ms (to indicate to device 0 that it is busy). Drive 1 shall then assert PDIAG- within 30 seconds to indicate that it is no longer busy and is able to provide status.

Following the receipt of a valid Execute Drive Diagnostics command, device 1 shall negate PDIAG- within 1 ms to indicate to device 0 that it is busy and has not yet passed its drive diagnostics. If device 1 is present then device 0 shall wait up to 6 seconds from the receipt of a valid Execute Drive Diagnostics command for drive 1 to assert PDIAG-. Device 1 should clear BSY before asserting PDIAG-, as PDIAG- is used to indicate that device 1 has passed its diagnostics and is ready to post status.

If device 1 did not assert DASP- during reset initialization, device 0 shall post its own status immediately after it completes diagnostics and clear the device 1 Status register to 00h. Device 0 may be unable to accept commands until it has finished its reset procedure and is ready (DRDY=1).

Device 1 shall release PDIAG-/CBLID- no later than after the first command following a power on or hardware reset sequence so that the host may sample PDIAG-/CBLID- in order to detect the presence or absence of an 80-conductor cable assembly.

CSEL (Cable Select)

The drive is configured as either Device 0 or 1 depending upon the value of CSEL.

- If CSEL is grounded, the device address is 0
- If CSEL is open, the device address is 1

KEY

Pin position 20 has no connection pin. It is recommended to close the respective position of the cable connector in order to avoid incorrect insertion.

IORDY

This signal is negated to extend the host transfer cycle when a drive is not ready to respond to a data transfer request and may be negated when the host transfer cycle is less than 240 ns for PIO data transfer. This signal is an open-drain output with 24 mA sink capability and an external resistor is needed to pull this line to 5 volts.

DMACK-

This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.

This signal is internally pulled up to 5 Volt through a 15kΩ resistor with a resistor tolerance value of –50% to +100%.

DMARQ

This signal is used for DMA data transfers between the host and drive. It shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW- signals. This signal is used in a handshake mode with DMACK-. This signal is a 3-state line with 24 mA sink capability and internally pulled down to GND through a 10 kΩ resistor.

HDMARDY- (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive. The signal HDMARDY- is a flow control signal for Ultra DMA data in bursts. This signal is held asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data in transfers. The host may negate HDMARDY- to pause an Ultra DMA data in transfer.

HSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The signal HSTROBE is the data out strobe signal from the host for an Ultra DMA data out transfer. Both the rising and falling edge of HSTROBE latch the data from DD (15:0) into the device. The host may stop toggling HSTROBE to pause an Ultra DMA data out transfer.

STOP (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The STOP signal shall be asserted by the host prior to initiation of an Ultra DMA burst. A STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during or after data transfer in an Ultra DMA mode signals the termination of the burst.

DDMARDY- (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The signal DDMARDY- is a flow control signal for Ultra DMA data out bursts. This signal is held asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data out transfers. The device may negate DDMARDY- to pause an Ultra DMA data out transfer.

DSTROBE (Ultra DMA)

This signal is used only for Ultra DMA data transfers between host and drive.

The signal DSTROBE is the data in strobe signal from the device for an Ultra DMA data in transfer. Both the rising and the falling edge of DSTROBE latch the data from DD (15:0) into the host. The device may stop toggling DSTROBE to pause an Ultra DMA data in transfer.

Device termination

The termination resistors on the device side are implemented on the drive side as follows:

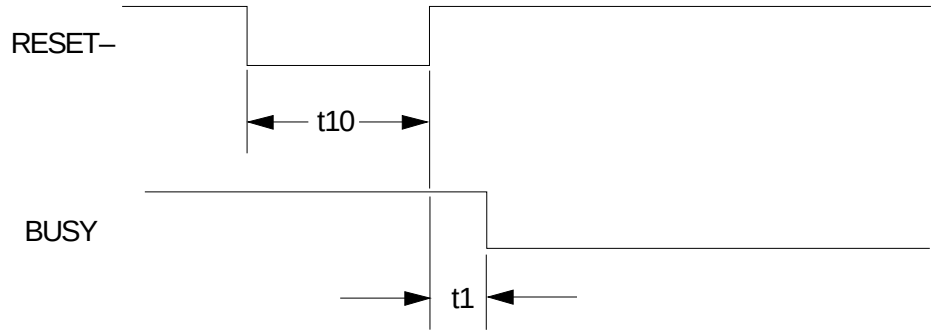
- 33 Ω for DD0 through DD15, DMARQ, INTRQ
- 82 Ω for CS0-, CS1-, DA0, DA1, DA2, DIOR-, DIOW-, DMACK-
- 22 Ω for IORDY

7.4 Interface logic signal levels

The interface logic signals have the following electrical specifications:

Inputs	Input High Voltage	2.0 V min
	Input Low Voltage	–0.8 V max.
Outputs:	Output High Voltage	2.4 V min.
	Output Low Voltage	0.5 V max.

7.5 Reset timings

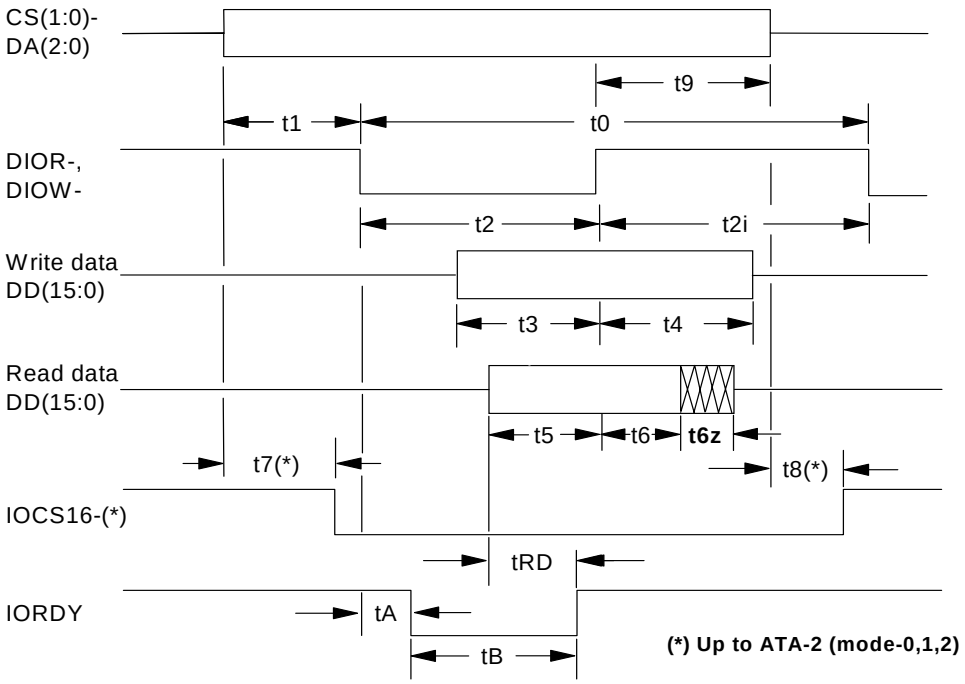


	PARAMETER DESCRIPTION	Min (µs)	Max (µs)
t10	RESET low width	25	-
t14	RESET high to not BUSY	-	31

Figure 1: System reset timing

7.6 PIO timings

The PIO cycle timings meet Mode 4 of the ATA/ATAPI-6 description.



	PARAMETER DESCRIPTION	MIN (ns)	MAX (ns)
t0	Cycle time	120	–
t1	Address valid to DIOR-/DIOW- setup	25	–
t2	DIOR-/DIOW- pulse width	70	–
t2i	DIOR-/DIOW- recovery time	25	–
t3	DIOW- data setup	20	–
t4	DIOW- data hold	10	–
t5	DIOR- data setup	20	–
t6	DIOR- data hold	5	–
t9	DIOR-/DIOW- to address valid hold	10	–
tA	IORDY setup width	–	35
tB	IORDY pulse width	–	1250

Figure 2: PIO cycle timings

7.6.1 Write DRQ interval time

For write sectors and write multiple operations 3.8 ms is inserted from the end of negation of the DRQ bit until setting of the next DRQ bit.

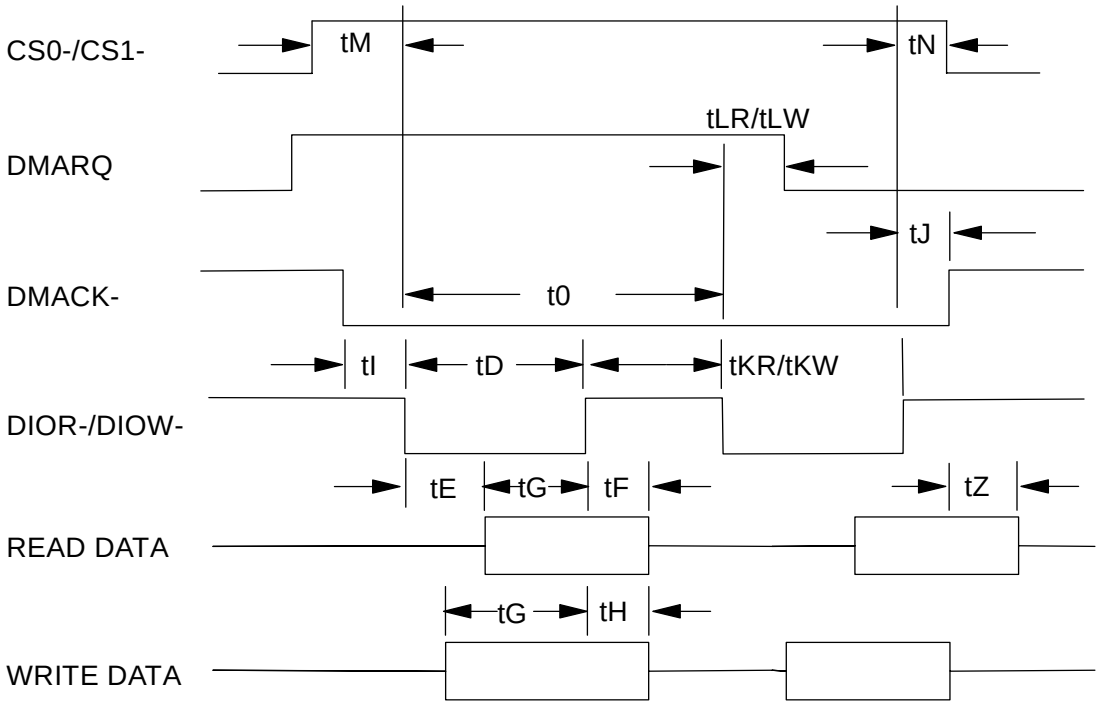
7.6.2 Read DRQ interval time

For read sectors and read multiple operations the interval from the end of negation of the DRQ bit until setting of the next DRQ bit is as follows:

- In the event that a host reads the status register only before the sector or block transfer DRQ interval, the DRQ interval 4.2 µs
- In the event that a host reads the status register after or both before and after the sector or block transfer, the DRQ interval is 11.5 µs

7.7 Multi word DMA timings

The Multiword DMA timings meet Mode 2 of the ATA/ATAPI-6 description.



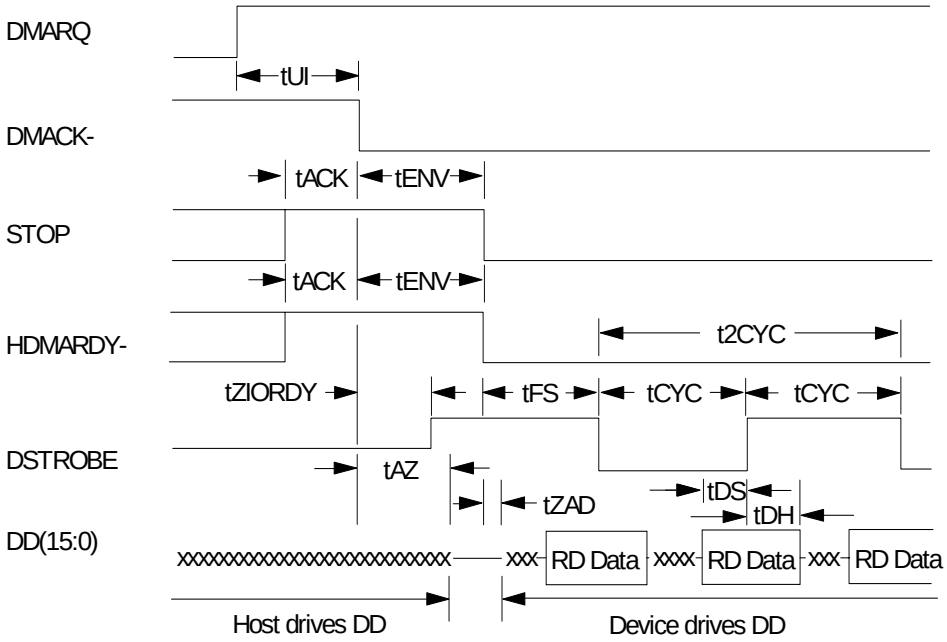
	PARAMETER DESCRIPTION	MIN (ns)	MAX (ns)
t0	Cycle time	120	–
tD	DIOR-/DIOW- asserted pulse width	70	–
tE	DIOR- data access	–	50
tF	DIOR- data hold	5	–
tG	DIOR-/DIOW- data setup	20	–
tH	DIOW- data hold	10	–
tI	DMACK- to -DIOR-/DIOW- setup	0	–
tJ	DIOR-/DIOW- to DMACK- hold	5	–
tKR/tKW	DIOR-/DIOW- negated pulse width	25	–
tLR/tLW	DIOR-/DIOW- to DMARQ- delay	–	35
tM	CS (1:0) valid to DIOR-/DIOW-	25	-
tN	CS (1:0)	10	-
tZ	DMACK- to read data released	–	25

Figure 3: Multiword DMA cycle timings

7.8 Ultra DMA timings

The Ultra DMA timings meet Mode 0, 1, 2, and 4 of the Ultra DMA Protocol.

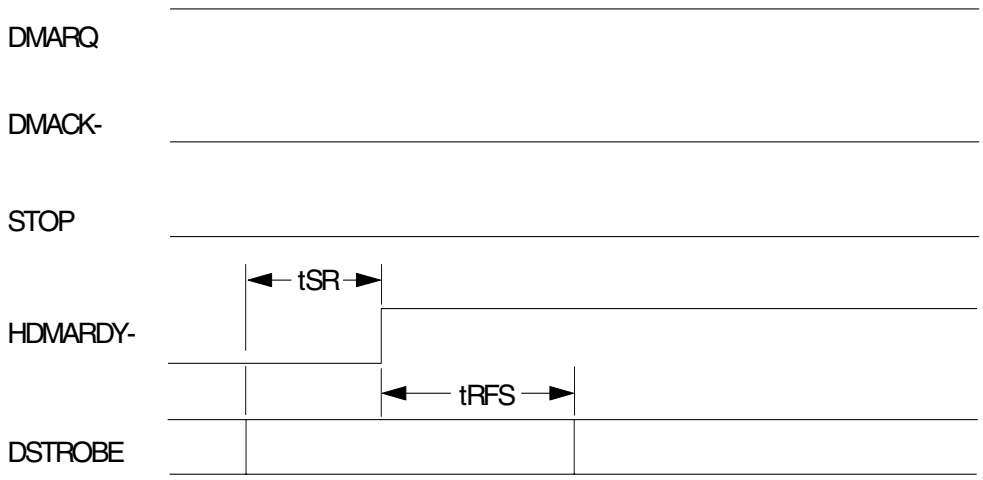
7.8.1 Initiating Read DMA



	PARAMETER DESCRIPTION (all values in ns)	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tUI	Unlimited interlock time	0	–	0	–	0	0	0	–	0	–	0	–
tACK	Setup time for DMACK-	20	–	20	–	20	–	20	–	20	–	20	–
tENV	Envelope time	20	70	20	70	20	70	20	55	20	55	20	50
tZIORDY	Minimum time before driving IORDY	0	–	0	–	0	–	0	–	0	–	0	–
tFS	First DSTROBE time	0	230	0	200	0	170	0	130	0	120	–	90
tCYC	Cycle time	112	–	73	–	54	–	39	–	25	–	17	–
t2CYC	Two cycle time	230	–	154	–	115	–	86	–	57	–	38	–
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10		10
tZAD	Drivers to assert	0	–	0	–	0	–	0	–	0	–	0	–
tDS	Data setup time at host	15	–	10	–	7	–	7	–	5	–	4.8	–
tDH	Data hold time at host	5	–	5	–	5	–	5	–	5	–	4.8	–
tDZFS	Time from data ouput released-to-driving until the first transition of critical timing	70	–	48	–	31	–	20	–	6.7	–	25	–

Figure 4: Ultra DMA cycle timings (Initiating Read)

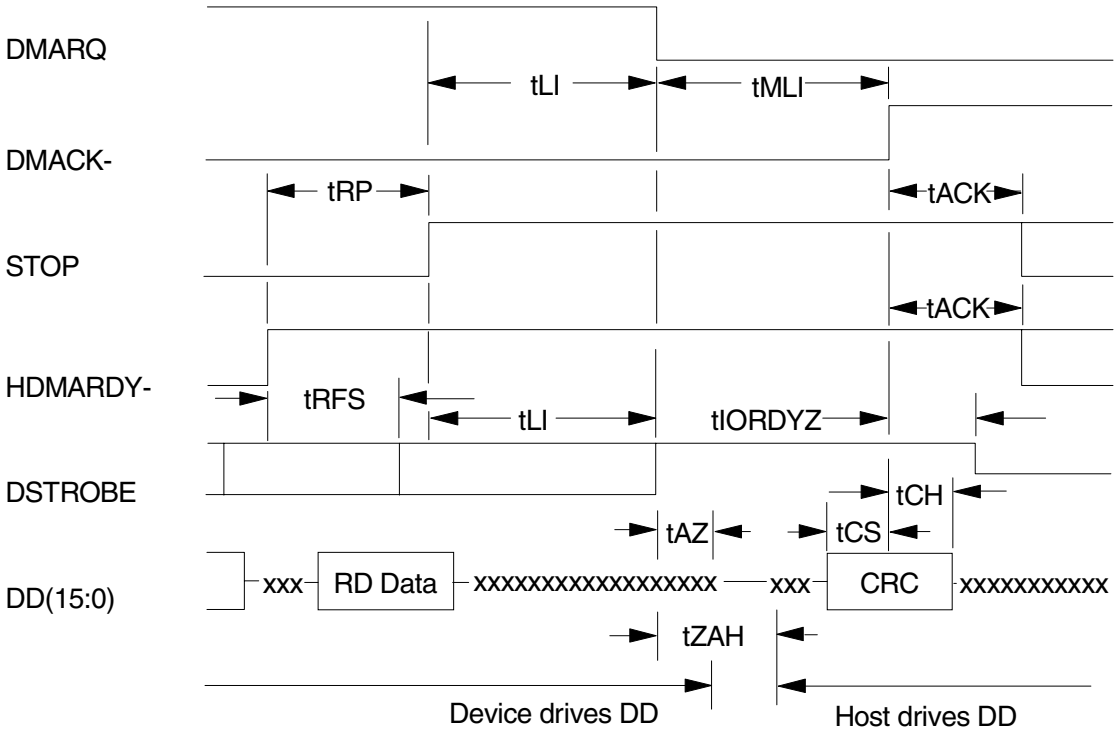
7.8.2 Host Pausing Read DMA



	PARAMETER DESCRIPTION (all values in ns)	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tSR	DSTROBE to HDMARDY- time	–	50	–	30	–	20	–	–	–	–	–	–
tRFS	HDMARDY- to final DSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50

Figure 5: Ultra DMA cycle timings (Host Pausing Read)

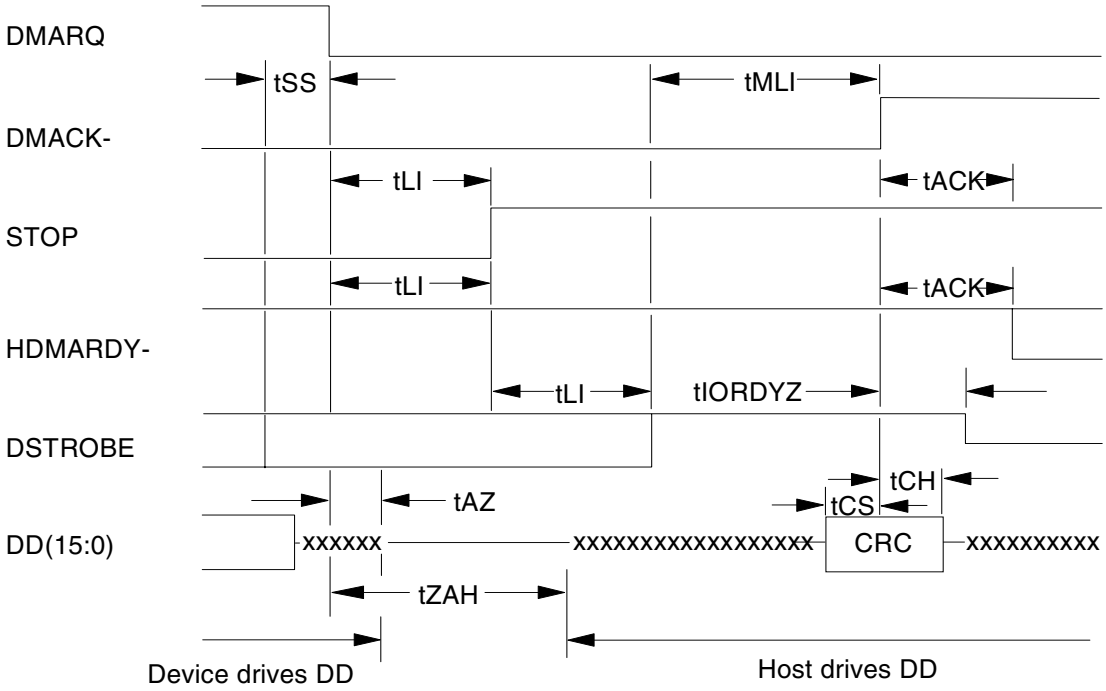
7.8.3 Host Terminating Read DMA



	PARAMETER DESCRIPTION (all values in ns)	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tRFS	HDMARDY- to final DSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	–	85	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10	–	10
tZAH	Minimum delay time required for output	20	–	20	–	20	–	20	–	20	–	20	–
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	20	–
tCS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–	5	–
tCH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK-	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20

Figure 6: Ultra DMA cycle timings (Host Terminating Read)

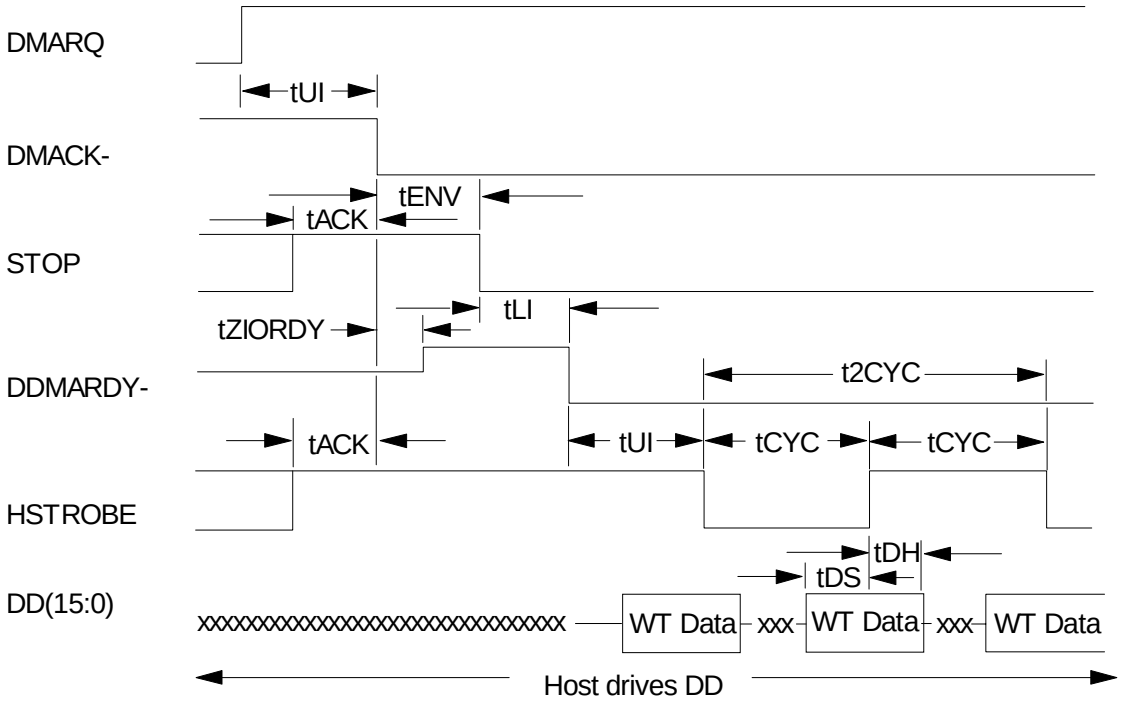
7.8.4 Device Terminating Read DMA



	PARAMETER DESCRIPTION (all values in ns)	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tSS	Time from DSTROBE edge to negation of DMARQ	50	–	50	–	50	–	50	–	50	–	50	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tAZ	Maximum time allowed for output drivers to release	–	10	–	10	–	10	–	10	–	10	–	10
tZAH	Maximum delay time required for output	20	–	20	–	20	–	20	–	20	–	20	–
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	20	–
tCS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–	5	–
tCH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK-	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20

Figure 12 : Ultra DMA cycle timings (Device Terminating Read)

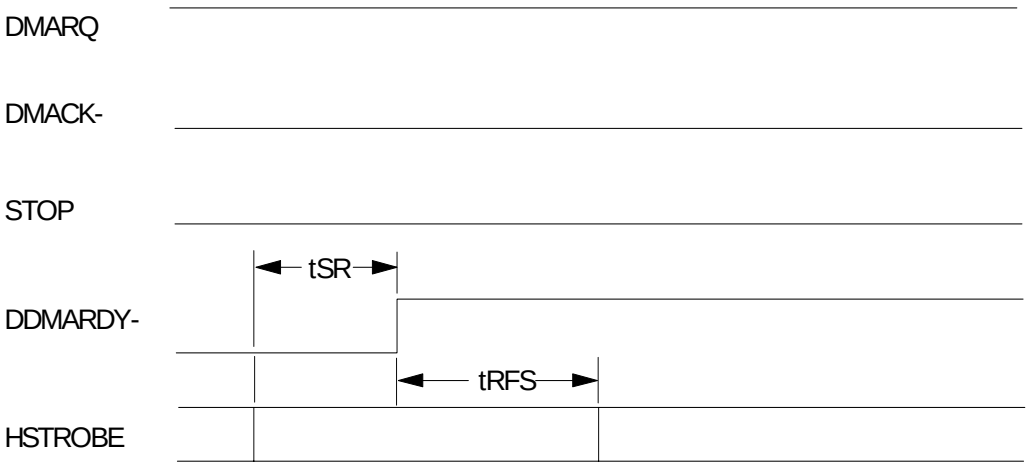
7.8.5 Initiating Write DMA



	PARAMETER DESCRIPTION (all values in ns)	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tUI	Unlimited interlock time	0	–	0	–	0	–	0	–	0	–	0	–
tACK	Setup time for DMACK-	20	–	20	–	20	–	20	–	20	–	20	–
tENV	Envelope time	20	70	20	70	20	70	20	55	20	55	20	55
tZIORDY	Minimum time before driving IORDY	0	–	0	–	0	–	0	–	0	–	0	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tCYC	Cycle time	112	–	73	–	54	–	39	–	25	–	16.8	–
t2CYC	Two cycle time	230	–	154	–	115	–	86	–	57	–	38	–
tDS	Data setup time at device	15	–	10	–	7	–	7	–	5	–	4	–
tDH	Data Hold time at device	5	–	5	–	5	–	5	–	5	–	4.6	–

Figure 13 : Ultra DMA cycle timing (Initiating Write)

7.8.6 Device Pausing Write DMA

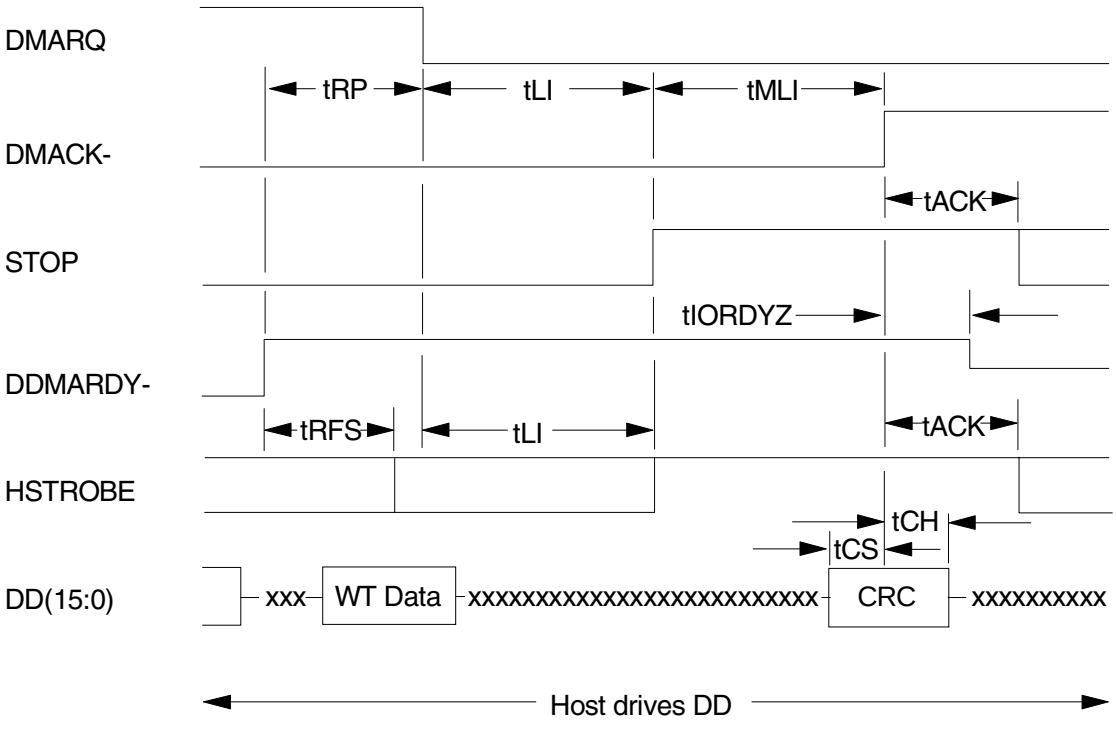


	PARAMETER DESCRIPTION (all values in ns)	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tSR	HSTROBE to DDMARDY- time	–	50	–	30	–	20	–	–	–	–	–	–
tRFS	DDMARDY- to final HSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50

Note: When a device does not satisfy the tSR timing, it shall be ready to receive two more strobes after DDMARDY– is negated.

Figure 7: Ultra DMA cycle timing (Device Pausing Write)

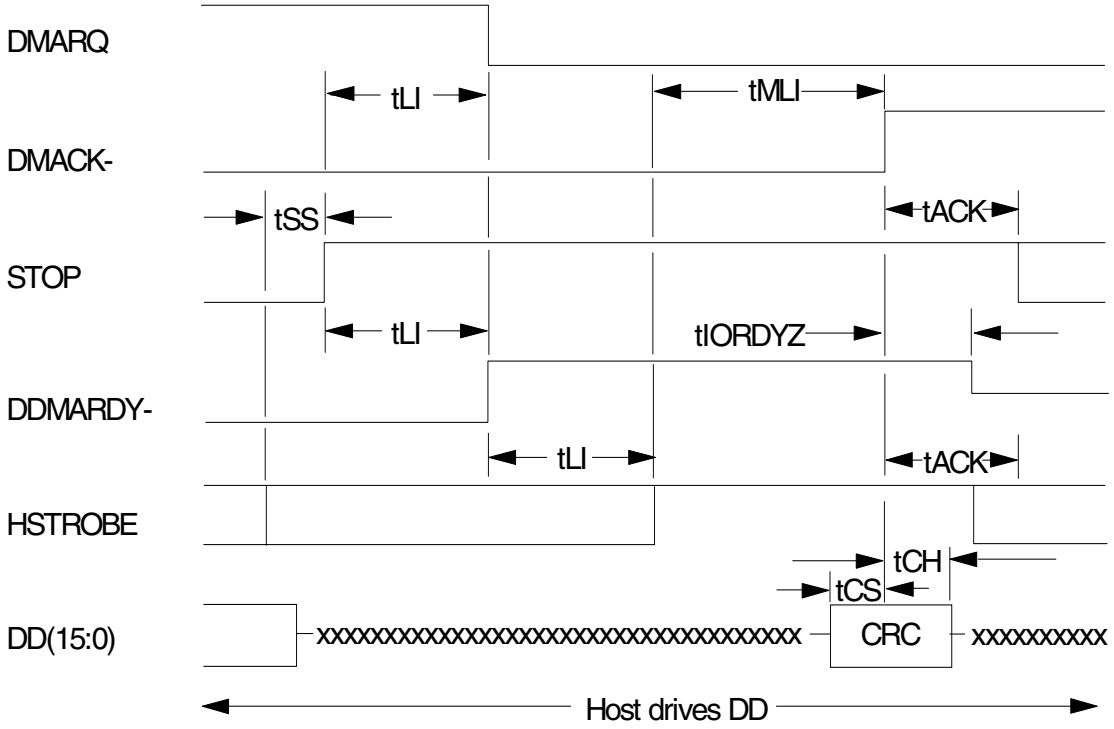
7.8.7 Device Terminating Write DMA



	PARAMETER DESCRIPTION (all values in ns)	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tRFS	DDMARDY- to final HSTROBE time	–	75	–	70	–	60	–	60	–	60	–	50
tRP	Ready to pause time	160	–	125	–	100	–	100	–	100	–	85	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tMLI	Interlocking time with minimum	20	–	20	–	20	–	20	–	20	–	20	–
tCS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–	5	–
tCH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK-negation	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20

Figure 8: Ultra DMA cycle timings (Device TerminatingWrite)

7.8.8 Host Terminating Write DMA



	PARAMETER DESCRIPTION (all values in ns)	MODE 0		MODE 1		MODE 2		MODE 3		MODE 4		MODE 5	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
tSS	Time from HSTROBE edge to assertion of STOP	50	–	50	–	50	–	50	–	50	–	50	–
tLI	Limited interlock time	0	150	0	150	0	150	0	100	0	100	0	75
tMLI	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	20	–
tCS	CRC word setup time at device	15	–	10	–	7	–	7	–	5	–	5	–
tCH	CRC word hold time at device	5	–	5	–	5	–	5	–	5	–	5	–
tACK	Hold time for DMACK-	20	–	20	–	20	–	20	–	20	–	20	–
tIORDYZ	Maximum time before releasing IORDY	–	20	–	20	–	20	–	20	–	20	–	20

Figure 9: Ultra DMA cycle timings (Host Terminating Write)

7.9 Addressing of registers

The host addresses the drive through a set of registers called a Task File. These registers are mapped into the host's I/O space. Two chip select lines (CS0– and CS1–) and three address lines (DA0–2) are used to select one of these registers, while a DIOR– or DIOW– is provided at the specified time.

The chip select line CS0- is used to address the Command Block registers while the CS1– is used to address Control Block registers.

The following table shows the I/ O address map.

Table 34: I/O address map

CS0–	CS1–	DA2	DA1	DA0	DIOR– = 0 (Read)	DIOW– = 0 (Write)
					Command Block Registers	
0	1	0	0	0	Data Reg.	Data Reg.
0	1	0	0	1	Error Reg.	Features Reg.
0	1	0	1	0	Sector count Reg.	Sector count Reg.
0	1	0	1	1	Sector number Reg.	Sector number Reg.
0	1	1	0	0	Cylinder low Reg.	Cylinder low Reg.
0	1	1	0	1	Cylinder high Reg.	Cylinder high Reg.
0	1	1	1	0	Drive/Head Reg.	Drive/Head Reg.
0	1	1	1	1	Status Reg.	Command Reg.
					Control Block Registers	
1	0	1	1	0	Alt. Status Reg.	Device control Reg.

Note: "Addr" field is shown as an example.

During DMA operation (from writing to the command register until an interrupt) not all registers are accessible. For example, the host is not supposed to read status register contents before interrupt (the value is invalid).

7.9.1 Cabling

The maximum cable length from the host system to the drive plus circuit pattern length in the host system shall not exceed 18 inches.

For higher data transfer application (>8.3 MB/s) a modification in the system design is recommended to reduce cable noise and cross-talk, such as a shorter cable, bus termination, or a shielded cable.

For systems operating with Ultra DMA mode 3, 4, and 5, 80-conductor ATA cable assembly (SFF-8049) shall be used

Part 2. Interface specification

8.0 General

8.1 Introduction

This specification describes the host interface of the HDS7225xxVLATx0 hard disk drive.

The interface conforms to the Working Document of Information technology, AT Attachment with Packet Interface Extension (ATA/ATAPI-6) Revision 3b, dated 26 February 2002, with certain limitations described in Section 8.3 below.

8.2 Terminology

Device	The HDS7225xxVLATx0 hard disk drive
Host	The system to which the device is attached

8.3 Deviations from standard

The device conforms to the referenced specifications with the following deviations:

Check Power Mode. Check Power Mode command returns FFh to Sector Count Register when the device is in Idle mode. This command does not support 80h as the return value.

H**ard Reset.** Hard reset response is not the same as that of power on reset. Refer to section 10.1, “Reset response” on page 73 for details.

9.0 Registers

9.1 Register set

Table 35: Register Set

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	READ (DIOR-)	WRITE (DIOW-)
N	N	x	x	x	Data bus high impedance	Not used
					Control block registers	
N	A	0	x	x	Data bus high impedance	Not used
N	A	1	0	x	Data bus high impedance	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	Device Address	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error Register	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	0	1	1	* LBA bits 0-7	* LBA bits 0-7
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	0	* LBA bits 8-15	* LBA bits 8-15
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	0	1	* LBA bits 16-23	* LBA bits 16-23
A	N	1	1	0	Device/Head.	Device/Head
A	N	1	1	0	* LBA bits 24-27	* LBA bits 24-27
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

Logic conventions: A = signal asserted
N = signal not asserted
x = either A or N

* = Mapping of registers in LBA mode

Communication to or from the device is through an I/O Register that routes the input or output data to or from the registers addressed by the signals from the host(CS0-, CS1-, DA2, DA1, DA0, DIOR- and DIOW-).

The Command Block Registers are used for sending commands to the device or posting status from the device.

The Control Block Registers are used for device control and to post alternate status.

9.2 Alternate Status Register

Table 36: Alternate Status Register

7	6	5	4	3	2	1	0
BSY	RDY	DF	DSC/ SERV	DRQ	COR	IDX	ERR

This register contains the same information as the Status Register. The only difference between this register and the Status Register is that reading the Alternate Status Register does not imply an interrupt acknowledge or a clear of a pending interrupt. See section 9.14 ‘Status Register” on page 70 for the definition of the bits in this register.

9.3 Command Register

This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The command set is shown in Table 48: ‘Command Set (1 of 2)” on page 105 and Table 49: ‘Command Set (2 of 2)” on page 106. All other registers required for the command must be set up before writing to the Command Register.

9.4 Cylinder High Register

This register contains the high order bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 16–23. At the end of the command, this register is updated to reflect the current LBA Bits 16–23.

The cylinder number may be from zero to the number of cylinders minus one.

When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 16-23 and the "previous content" contains Bits 40-47. The 48-bit Address feature set is described in Section 9.16, "48-Bit Address Feature Set" on page 93.

9.5 Cylinder Low Register

This register contains the low order 8 bits of the starting cylinder address for any disk access. At the end of the command, this register is updated to reflect the current cylinder number.

In LBA Mode this register contains Bits 8–15. At the end of the command, this register is updated to reflect the current LBA Bits 8–15.

The cylinder number may be from zero to the number of cylinders minus one (1).

When 48-bit addressing commands are used, the "most recently written" content contains LBA Bits 8-15 and the "previous content" contains Bits 32-39.

9.6 Data Register

This register is used to transfer data blocks between the device data buffer and the host. It is also the register through which sector information is transferred on a Format Track command and the configuration information is transferred on an Identify Device command.

All data transfers are 16 bits wide, except for ECC byte transfers, which are 8 bits wide. Data transfers are PIO only.

The register contains valid data only when DRQ = 1 is in the Status Register.

9.7 Device Control Register

Table 37: Device Control Register

7	6	5	4	3	2	1	0
HOB	-	-	-	1	SRST	-IEN	0

Bit	Definitions
HOB	HOB (high order byte) is defined by the 48-bit Address feature set. A write to any Command Register shall clear the HOB bit to zero.
SRST	Software Reset. The device is held at reset when RST = 1. Setting RST = 0 again enables the device. To ensure that the device recognizes the reset, the host must set RST = 1 and wait for at least 5 ms before setting RST = 0.
-IEN	Interrupt Enable. When IEN = 0, and the device is selected, the device interrupts to the host will be enabled. When IEN = 1, or the device is not selected, the device interrupts to the host will be disabled.

9.8 Drive Address Register

Table 38: Drive Address Register

7	6	5	4	3	2	1	0
HIZ	-WTG	-H3	-H2	-H1	-H0	-DS1	-DS0

This register contains the inverted drive select and head select addresses of the currently selected drive.

Bit	Definitions
HIZ	High Impedance. This bit is not a device and will always be in a high impedance state.
-WTG	Write Gate. This bit is 0 when writing to the disk device is in progress.
-H3, -H2,-H1,-H0-	-Head Select. These four bits are the one's complement of the binary coded address of the currently selected head. Bit -H0 is the least significant.
-DS1	Drive Select 1. The Drive Select bit for device 1 is active low. DS1 = 0 when device 1 (slave) is selected and active.
-DS0	Drive Select 0. The Drive Select bit for device 0 is active low. DS0 = 0 when device 0 (master) is selected and active.

9.9 Device/Head Register

Table 39: Device Head/Register

7	6	5	4	3	2	1	0
1	L	1	DRV	HS3	HS2	HS1	HS0

This register contains the device and head numbers.

Bit	Definitions
L	Binary encoded address mode select. When L = 0, addressing is by CHS mode. When L = 1, addressing is by LBA mode.
DRV	Device. When DRV = 0, device 0 (master) is selected. When DRV = 1, device 1 (Slave) is selected.
HS3, HS2, HS1, HS0	Head Select. These four bits indicate the binary encoded address of the head. Bit HS0 is the least significant bit. At command completion, these bits are updated to reflect the currently selected head. The head number may be from zero to the number of heads minus one. In LBA mode, HS3 through HS0 contain bits 24–27 of the LBA. At command completion these bits are updated to reflect the current LBA bits 24–27.

9.10 Error Register

Table 40: Error Register

7	6	5	4	3	2	1	0
CRC	UNC	0	IDNF	0	ABRT	TK0NF	AMNF

This register contains the status from the last command executed by the device or a diagnostic code. At the completion of any command, except Execute Device Diagnostic, the contents of this register are always valid even if ERR = 0 is in the Status Register.

Following a power on, a reset, or completion of an Execute Device Diagnostic command, this register contains a diagnostic code. See Table 44: ‘Diagnostic codes” on page 74 for the definitions.

Bit	Definitions
ICRCE (CRC)	Interface CRC Error. When CRC = 1, it indicates that a CRC error has occurred on the data bus during a Ultra DMA transfer.
UNC	Uncorrectable Data Error. When UNC = 1 it indicates that an uncorrectable data error has been encountered.
IDNF (IDN)	ID Not Found. When IDN = 1, it indicates that the requested sector's ID field could not be found.
ABRT (ABT)	Aborted Command. When ABT = 1, it indicates that the requested command has been aborted due to a device status error or an invalid parameter in an output register.
TK0NF (T0N)	Track 0 Not Found. When T0N = 1, it indicates that track 0 was not found during a Recallibrate command.
AMNF (AMN)	Address Mark Not Found. When AMN = 1, it indicates that the data address mark has not been found after finding the correct ID field for the requested sector.

9.11 Features Register

This register is command specific. It is used with the Set Features command, the S.M.A.R.T. Function Set command, and the Format Unit command.

9.12 Sector Count Register

This register contains the number of sectors of data requested to be transferred on a read or write operation between the host and the device. If the value in the register is set to 0, a count of 256 sectors (in 28-bit addressing) or 65,536 sectors (in 48-bit addressing) is specified.

If the register is zero at command completion, the command was successful. If it is not successfully completed, the register contains the number of sectors which need to be transferred in order to complete the request.

The contents of the register are defined otherwise on some commands. These definitions are given in the command descriptions.

9.13 Sector Number Register

This register contains the starting sector number for any disk data access for the subsequent command. The sector number is from one to the maximum number of sectors per track.

In LBA mode, this register contains Bits 0–7. At the end of the command this register is updated to reflect the current LBA Bits 0–7.

When 48-bit commands are used, the "most recently written" content contains LBA Bits 0-7 and the "previous content" contains Bits 24-31.

9.14 Status Register

Table 41: Status Register

7	6	5	4	3	2	1	0
BSY	DRDY	DF	DSC/ SERV	DRQ	CORR	IDX	ERR

This register contains the device status. The contents of this register are updated whenever an error occurs and at the completion of each command.

If the host reads this register when an interrupt is pending, it is considered to be the interrupt acknowledge. Any pending interrupt is cleared whenever this register is read.

If BSY=1, no other bits in the register are valid.

Bit	Definitions
BSY	Busy. Bit BSY=1 whenever the device is accessing the registers. The host should not read or write any registers when BSY=1. If the host reads any register when BSY=1, the contents of the Status Register will be returned.
DRDY (RDY)	Device Ready. RDY=1 indicates that the device is capable of responding to a command. RDY will be set to zero during power on until the device is ready to accept a command. If the device detects an error while processing a command, RDY is set to zero until the Status Register is read by the host, at which time RDY is set back to one.
DF	Device Fault. This product does not support DF bit. DF is always zero.
DSC	Device Seek Complete. If DSC=1, it indicates that a Seek has completed and the device head is settled over a track. Bit DSC is set to 0 by the device just before a Seek begins. When an error occurs, this bit is not changed until the Status Register is read by the host at which time the bit again indicates the current Seek complete status. When the device enters into or is in Standby mode or Sleep mode, this bit is set by the device in spite of the drive not spinning up.
DRQ	Data Request. Bit DRQ=1 indicates that the device is ready to transfer a word or byte of data between the host and the device. The host should not write the Command register when DRQ=1.
CORR (COR)	Corrected Data. Always 0
IDX	Index. IDX=1 once per revolution. Because IDX=1 only for a very short time during each revolution, the host may not see it set to 1 even if the host is continuously reading the Status Register. Therefore the host should not attempt to use IDX for timing purposes.
ERR	Error. ERR=1 indicates that an error occurred during execution of the previous command. The Error Register should be read to determine the error type. The device sets bit ERR=0 when the next command is received from the host.

10.0 General operation

10.1 Reset response

ATA has the following three types of resets:

Power On Reset (POR)	The device executes a series of electrical circuitry diagnostics, spins up the head disk assembly, tests speed and other mechanical parametric, and sets default values.
Hard Reset (Hardware Reset)	The RESET- signal is negated in the ATA Bus. The device resets the interface circuitry and sets the default values.
Soft Reset (Software Reset)	The SRST bit in the Device Control Register is set and then is reset. The device resets the interface circuitry according to the Set Features requirement.

The actions of each reset are shown in the table below.

Table 42: Reset response table

	POR	hard reset	soft reset
Aborting Host interface	-	O	O
Aborting Device operation	-	(*1)	(*1)
Initialization of hardware	O	X	X
Internal diagnostic	O	X	X
Spinning spindle	O	X	X
Initialization of registers (*2)	O	O	O
DASP handshake	O	O	X
PDIAG handshake	O	O	O
Reverting programmed parameters to default Number of CHS (set by Initialize Device Parameters) Multiple mode Write Cache Read look-ahead ECC bytes	O	(*3)	(*3)
Power mode	(*5)	(*4)	(*4)
Disable Standby timer(*5)	O	X	X

O – execute X – does not execute

Notes:

(*1) Execute after the data in write cache has been written.

(*2) The default value on POR is shown in Table 43: “Default Register Values” on page 74.

(*3) The Set Features command with Feature register = CCh enables the device to revert these parameters to the power on defaults.

(*4) In the case of Sleep mode, the device goes to Standby mode. In other cases, the device does not change current mode.

(*5) Idle when Power-Up in Standby feature set is disabled. Standby when Power-Up in Standby feature set is enabled.

10.2 Register initialization

After a power on, a hard reset, or a software reset, the register values are initialized as shown in the table below.

Table 43: Default Register Values

Register	Default Value
Error	Diagnostic Code
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	A0h
Status	50h
Alternate Status	50h

The meaning of the Error Register diagnostic codes resulting from power on, hard reset, or the Execute Device Diagnostic command is shown in the figure below.

Table 44: Diagnostic codes

Code	Description
01h	No error detected
02h	Formatter device error
03h	Sector buffer error
04h	ECC circuitry error
05h	Controller microprocessor error
8xh	Device 1 failed

10.3 Diagnostic and Reset considerations

For each Reset and Execute Device Diagnostic, the diagnostic is done as follows:

Power On Reset DASP– is read by Device 0 to determine if Device 1 is present. If Device 1 is present, Device 0 shall read PDIAG– to determine when it is valid to clear the BSY bit and whether Device 1 has powered on or reset without error, otherwise Device 0 clears the BSY bit whenever it is ready to accept commands. Device 0 may assert DASP– to indicate device activity.

Hard Reset, Soft Reset If Device 1 is present, Device 0 shall read PDIAG– to determine when it is valid to clear the BSY bit and whether Device 1 has reset without any errors; otherwise, Device 0 shall simply reset and clear the BSY bit. DASP– is asserted by Device 0 (and Device 1 if it is present) in order to indicate device active.

Execute Device Diagnostic If Device 1 is present, Device 0 shall read PDIAG– to determine when it is valid to clear the BSY bit and if Device 1 passed or failed the EXECUTE DEVICE DIAGNOSTIC command; otherwise, Device 0 shall simply execute its diagnostics and then clear the BSY bit. DASP– is asserted by Device 0 (and Device 1 if it is present) in order to indicate that the device is active.

In each case – Power On Reset [Hard Reset], Soft Reset, and the Execute Device Diagnostic command – the Device 0 Error register value is interpreted using the table below.

Table 45: Reset error register values

Device 1 present?	PDIAG- Asserted?	Device 0 Passed	Error Register
Yes	Yes	Yes	01h
Yes	Yes	No	0xh
Yes	No	Yes	81h
Yes	No	No	8xh
No	(not read)	Yes	01h
No	(not read)	No	0xh

The "x" indicates the appropriate Diagnostic Code for the Power on, RESET-, Soft Reset, or Device Diagnostic error.

10.4 Sector Addressing Mode

All addressing of data sectors recorded on the device's media is done by a logical sector address. The logical CHS address for HDS7225xxVLATx0 is different from the actual physical CHS location of the data sector on the disk media.

HDS7225xxVLATx0 supports both Logical CHS Addressing Mode and LBA Addressing Mode as the sector addressing mode.

The host system may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the L bit in the DEVICE/HEAD register. A host system must set the L bit to 1 if the host uses LBA Addressing mode.

10.4.1 Logical CHS addressing mode

The logical CHS addressing is made up of three fields: the cylinder number, the head number, and the sector number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation mode but cannot exceed 255 (0FFh). Heads are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 15 (0Fh). Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation mode but cannot exceed 65535 (0FFFFh).

When the host selects a CHS translation mode using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested mode.

The default CHS translation mode is described in the Identify Device Information. The current CHS translation mode also is described in the Identify Device Information.

10.4.2 LBA addressing mode

Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation mode currently in effect, the LBA address of a given logical sector does not change. The following formula is always true:

```
LBA = ((cylinder x heads_per_cylinder + heads) x sectors_per_track) + sector - 1
```

where heads_per_cylinder and sectors_per_track are the current translation mode values.

On LBA addressing mode the LBA value is set to the following register:

Device/Head	<- - - LBA bits 27–24
Cylinder High	<- - - LBA bits 23–16
Cylinder Low	<- - - LBA bits 15–8
Sector Number	<- - - LBA bits 7–0

10.5 Overlapped and queued feature

Overlap allows devices to perform a bus release so that the other device on the bus may be used. To perform a bus release the device clears both DRQ and BSY to zero. When selecting the other device during overlapped operations, the host shall disable interrupts via the nIEN bit on the currently selected device before writing the Device/Head register to select the other device.

The only commands that may be overlapped are

NOP (with 01h subcommand code)	(’00’h)
Read DMA Queued	(’C7’h)
Service	(’A2’h)
Write DMA Queued	(’CC’h)

For the READ DMA QUEUED and WRITE DMA QUEUED commands, the device may or may not perform a bus release. If the device is ready to complete the execution of the command, it may complete the command immediately. If the device is not ready to complete the execution of the command, the device may perform a bus release and complete the command via a service request.

Command queuing allows the host to issue concurrent commands to the same device. Only commands included in the overlapped feature set may be queued. If a queue exists when a non-queued command is received, the nonqueued command shall be aborted and the commands in the queue shall be discarded. The ending status shall be ABORT command and the results are indeterminate.

The maximum queue depth supported by a device is indicated in word 73 of Identify Device information.

A queued command shall have a Tag provided by the host in the Sector Count register to uniquely identify the command. When the device restores register parameters during the execution of the SERVICE command, this Tag shall be restored so that the host may identify the command for which status is being presented. If a queued command is issued with a Tag value that is identical to the Tag value for a command already in the queue, the entire queue is aborted including the new command. The ending status is ABORT command and the results are indeterminate. If any error occurs, the command queue is aborted.

When the device is ready to continue processing a bus released command and BSY and DRQ are both cleared to zero, the device requests service by setting SERV to one, setting a pending interrupt, and asserting INTRQ if selected and if nIEN is cleared to zero. SERV shall remain set until all commands ready for service have been serviced. The pending interrupt shall be cleared and INTRQ negated by a Status register read or a write to the Command register.

When the device is ready to continue processing a bus released command and BSY or DRQ is set to one (i.e., the device is processing another command on the bus), the device requests service by setting SERV to one. SERV shall remain set until all commands ready for service have been serviced. At command completion of the current command processing (i.e., when both BSY and DRQ are cleared to zero), the device shall process interrupt pending and INTRQ per the protocol for the command being completed. No additional interrupt shall occur due to other commands ready for service until after the SERV bit of the device has been cleared to zero.

When the device receives a new command while queued commands are ready for service, the device shall execute the new command and process interrupt pending and INTRQ per the protocol for the new command. If the queued commands ready for service still exist at command completion of this command, SERV remains set to one but no additional interrupt shall occur due to commands ready for service.

When queuing commands, the host shall disable interrupts via the nIEN bit before writing a new command to the Command register and may re-enable interrupts after writing the command. When reading status at command completion of a command, the host shall check the SERV bit since the SERV bit may be set because the device is ready for service associated with another queued command. The host receives no additional interrupt to indicate that a queued command is ready for service.

10.6 Power management features

The power management feature set permits a host to modify the behavior in a manner which reduces the power required to operate. The power management feature set provides a set of commands and a timer that enables a device to implement low power consumption modes.

HDS7225xxVLATx0 implements the following set of functions:

- A Standby timer
- Idle command
- Idle Immediate command
- Sleep command
- Standby command
- Standby Immediate command

10.6.1 Power mode

Sleep Mode	The lowest power consumption when the device is powered on occurs in Sleep Mode. When in Sleep Mode, the device requires a reset to be activated.
Standby Mode	The device interface is capable of accepting commands, but since the media may not be immediately accessible, there is a delay while waiting for the spindle to reach operating speed.
Idle Mode	In Idle Mode the device is capable of responding immediately to media access requests.
Active Mode	The device is executing a command or accessing the disk media with the read look-ahead function or the write cache function.

10.6.2 Power management commands

Check Power Mode	allows a host to determine if a device is currently in, going to, or leaving standby mode.
Idle, Idle Immediate	move a device to idle mode immediately from the active or standby modes. The idle command also sets the standby timer count and starts the standby timer.
Sleep	moves a device to sleep mode. The device's interface becomes inactive at the completion of the sleep command. A reset is required to move a device out of sleep mode. When a device exits sleep mode it will enter standby mode.
Standby, Standby Immediate	move a device to standby mode immediately from the active or idle modes. The standby command also sets the standby timer count.

10.6.3 Standby timer

The standby timer provides a method for the device to automatically enter standby mode from either active or idle mode following a host programmed period of inactivity. If the device is in the active or idle mode, the device waits for the specified time period and, if no command is received, the device automatically enters the standby mode.

If the value of the SECTOR COUNT register on Idle command or Standby command is set to 00h, the standby timer is disabled.

10.6.4 Interface capability for power modes

Each power mode affects the physical interface as defined in the following table:

Table 46: Power conditions

Mode	BSY	RDY	Interface active	Media
Active	x	x	Yes	Active
Idle	o	1	Yes	Active
Standby	o	1	Yes	Inactive
Sleep	x	x	No	Inactive

Ready (RDY) is not a power condition. A device may post ready at the interface even though the media may not be accessible.

10.7 S.M.A.R.T. Function

The intent of Self-monitoring, analysis, and reporting technology (S.M.A.R.T.) is to protect user data and prevent unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, S.M.A.R.T. devices employ sophisticated data analysis algorithms to predict the likelihood of near-term degradation or fault condition. By alerting the host system of a negative reliability status condition, the host system can warn the user of the impending risk of a data loss and advise the user of appropriate action.

10.7.1 Attributes

Attributes are the specific performance or calibration parameters that are used in analyzing the status of the device. Attributes are selected by the device manufacturer based on that attribute's ability to contribute to the prediction of degrading or faulty conditions for that particular device. The specific set of attributes being used and the identity of these attributes is vendor specific and proprietary.

10.7.2 Attribute values

Attribute values are used to represent the relative reliability of individual performance or calibration attributes. The valid range of attribute values is from 1 to 253 decimal. Higher attribute values indicate that the analysis algorithms being used by the device are predicting a lower probability of a degrading or faulty condition existing. Accordingly, lower attribute values indicate that the analysis algorithms being used by the device are predicting a higher probability of a degrading or faulty condition.

10.7.3 Attribute thresholds

Each attribute value has a corresponding attribute threshold limit which is used for direct comparison to the attribute value to indicate the existence of a degrading or faulty condition. The numerical value of the attribute thresholds are determined by the device manufacturer through design and reliability testing and analysis. Each attribute threshold represents the lowest limit to which its corresponding attribute value can be equal while still retaining a positive reliability status. Attribute thresholds are set at the device manufacturer's factory and cannot be changed in the field. The valid range for attribute thresholds is from 1 through 253 decimal.

10.7.4 Threshold exceeded condition

If one or more attribute values, whose Pre-failure bit of their status flag is set, are less than or equal to their corresponding attribute thresholds, the device reliability status is negative, indicating an impending degrading or faulty condition.

10.7.5 S.M.A.R.T. commands

The S.M.A.R.T. commands provide access to attribute values, attribute thresholds, and other logging and reporting information.

10.7.6 Off-line read scanning

The device provides the off-line read scanning feature with reallocation. This is the extension of the off- line data collection capability. The device performs the entire read scan with reallocation of the marginal sectors to prevent loss of user data.

If interrupted by the host during the read scanning, the device services the host command.

10.7.7 Error log

Logging of reported errors is supported. The device provides information on the last five errors that the device reported as described in the SMART error log sector. The device may also provide additional vendor specific information on these reported errors. The error log is not disabled when SMART is disabled. Disabling SMART disables the delivering of error log information via the SMART READ LOG SECTOR command.

If a device receives a firmware modification, all error log data is discarded and the device error count for the life of the device is reset to zero.

10.7.8 Self-test

The device provides the self-test features which are initiated by SMART Execute Off-line Immediate

command. The self-test checks the fault of the device, reports the test status in Device Attributes Data, and stores the test result in the SMART self-test log sector as described in the SMART self-test log data structure. All SMART attributes are updated accordingly during the execution of self-test.

If it is interrupted by the host during the self-tests, the device services the host command.

If the device receives a firmware modification, all self-test log data is discarded

10.8 Security Mode Feature Set

Security Mode Feature Set is a powerful security feature. With a device lock password, a user can prevent unauthorized access to a device even if it is removed from the computer.

New commands are supported for this feature as listed below:

Security Set Password	('F1'h)
Security Unlock	('F2'h)
Security Erase Prepare	('F3'h)
Security Erase Unit	('F4'h)
Security Freeze Lock	('F5'h)
Security Disable Password	('F6'h)

10.8.1 Security mode

The following security modes are provided:

Device Locked Mode	The device disables media access commands after power on. Media access commands are enabled by either a Security Unlock command or a Security Erase Unit command.
Device Unlocked Mode	The device enables all commands. If a password is not set this mode is entered after power on, otherwise it is entered by a Security Unlock or a Security Erase Unit command.
Device Frozen Mode	The device enables all commands except those which can update the device lock function, set/change password. The device enters this mode via a Security Freeze Lock command. It cannot quit this mode until power off.

10.8.2 Security level

The following security levels are provided:

High level security	When the device lock function is enabled and the User Password is forgotten, the device can be unlocked via a Master Password.
Maximum level security	When the device lock function is enabled and the User Password is forgotten, only the Master Password with a Security Erase Unit command can unlock the device. User data is then erased.

10.8.3 Passwords

This function can have two types of passwords as described below.

Master Password	When the Master Password is set, the device does NOT enable the Device Lock Function, and the device CANNOT be locked with the Master Password, but the Master Password can be used for unlocking the locked device. Identify Device Information word 92 contains the value of the Master Password Revision Code set when the Master Password was last changed. Valid values are 0001h through FFFEh.
User Password	The User Password should be given or changed by a system user. When the User Password is set, the device enables the Device Lock Function, and the device is then locked on the next power on reset or hard reset.

The system manufacturer or dealer who intends to enable the device lock function for end users must set the master password even if only single level password protection is required.

10.8.4 Operation example

10.8.4.1 Master Password setting

The system manufacturer or dealer can set a new Master Password from default Master Password using the Security Set Password command without enabling the Device Lock Function.

The Master Password REvision Code is set to FFFEh as shipping default by the drive manufacturer.

10.8.4.2 User Password setting

When a User Password is set, the device will automatically enter lock mode the next time the device is powered on.

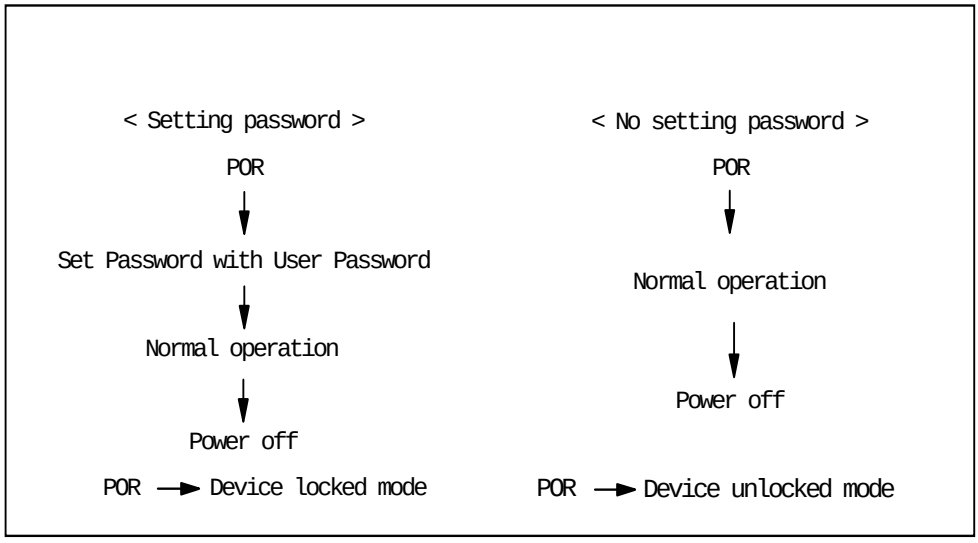


Figure 14 : Initial setting

10.8.4.3 Operation from POR after user password is set

When Device Lock Function is enabled, the device rejects media access command until a Security Unlock command is successfully completed.

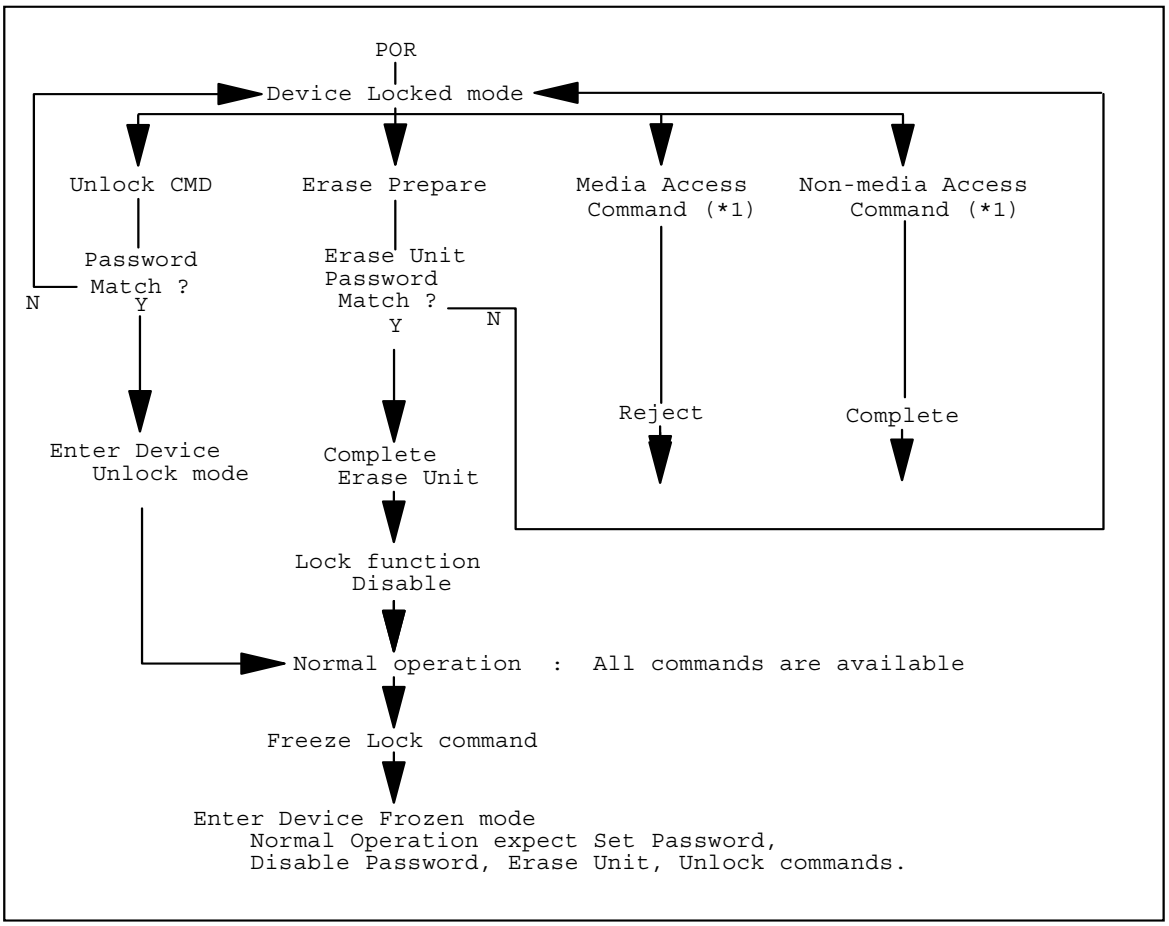


Figure 15 : Usual operation for POR

(*1) — refer to the commands in Figure 10.8.5, “Command table” on page 86.

10.8.4.4 User Password lost

If the User Password is forgotten and High level security is set, the system user cannot access any data. However the device can be unlocked using the Master Password.

If a system user forgets the User Password and Maximum security level is set, data access is impossible. However the device can be unlocked using the Security Erase Unit command to unlock the device and erase all user data with the Master Password.

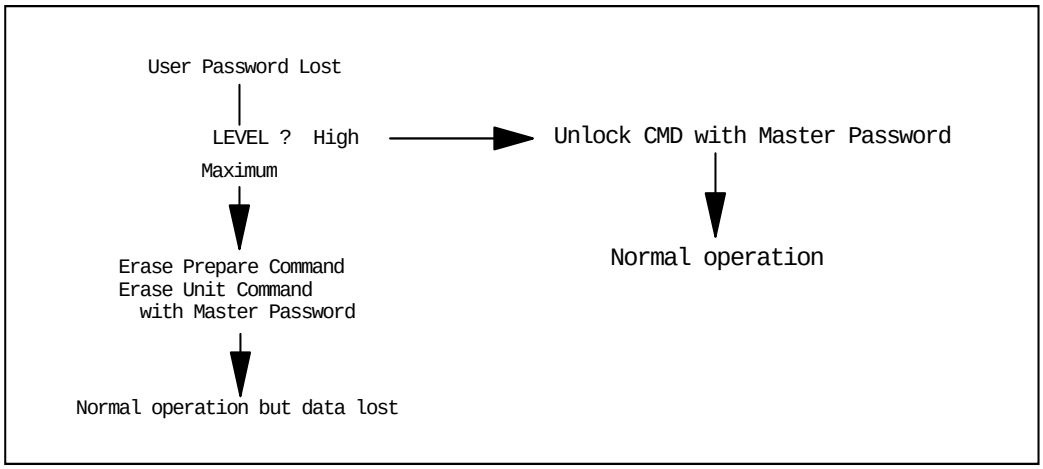


Figure 16 : Password lost

10.8.4.5 Attempt limit for the SECURITY UNLOCK command

The SECURITY UNLOCK command has an attempt limit, the purpose of which is to prevent attempts to unlock the drive with various passwords numerous times.

The device counts the password mismatch. If the password does not match, the device counts it without distinguishing the Master password and the User password. If the count reaches 5, EXPIRE bit (bit 4) of Word 128 in Identify Device information is set, and then the SECURITY ERASE UNIT command and the SECURITY UNLOCK command are aborted until a hard reset or a power off. The count and EXPIRE bit are cleared after a power on reset or a hard reset.

10.8.5 Command table

This table shows the device's response to commands when the Security Mode Feature Set (Device lock function) is enabled.

Table 47: Command table for device lock operation

Command	Device Mode				Command	Device Mode		
	Locked	Unlocked	Frozen			Locked	Unlocked	Frozen
Check Power Mode	o	o	o		Security Set Password	x	o	x
Execute Device Diagnostic	o	o	o		Security Unlock	o	o	x
Device Configuration RESTORE	x	o	o		Seek	o	o	o
Device Configuration FREEZE LOCK	o	o	o		Service	x	o	o
Device Configuration IDENTIFY	o	o	o		Set Features	o	o	o
Device Configuration SET	x	o	o		Set Max ADDRESS	x	o	o
Flush Cache	o	o	o		Set Max ADDRESS Ext	x	o	o
Flush Cache Ext	o	o	o		Set Multiple Mode	o	o	o
Format Track	x	o	o		Sleep	o	o	o
Identify Device	o	o	o		S.M.A.R.T. Disable Operations	o	o	o
Idle	o	o	o		S.M.A.R.T. Enable/Disable Attribute Autosave	o	o	o
Idle Immediate	o	o	o		S.M.A.R.T. Enable Operations	o	o	o
Initialize Device Parameters	o	o	o		S.M.A.R.T. Exectue Off-line Immdeiate	o	o	o
NOP					S.M.A.R.T. Read Attribute Values	o	o	o
Read Buffer	o	o	o		S.M.A.R.T. Read Attribute Thresholds	o	o	o
Read DMA	x	o	o		S.M.A.R.T. Return Status	o	o	o
Read DMA Ext	x	o	o		S.M.A.R.T. Save Attributre Values	o	o	o
Read DMA Queued	x	o	o		S.M.A.R.T. Read Log Sector	o	o	o
Read DMA Queued Ext	x	o	o		S.M.A.R.T. Write Log Sector	o	o	o
Read Log Ext	x	o	o		S.M.A.R.T. Enable/Disable Automatic Off-Line	o	o	o
Read Long	x	o	o		Standby	o	o	o
Read Multiple	x	o	o		Standby Immediate	o	o	o
Read Multiple Ext	x	o	o		Write Buffer	o	o	o
Read Native Max ADDRESS	o	o	o		Write DMA	x	o	o
Read Native Max Ext	o	o	o		Write DMA Ext	x	o	o
Read Sector(s)	x	o	o		Write DMA Queued	x	o	o
Read Sector(s) Ext	x	o	o		Write DMA Queued Ext	x	o	o
Read Verify Sector(s)	x	o	o		Write Log Ext	x	o	o
Read Verify Sector(s) Ext	x	o	o		Write Long	x	o	o
Recalibrate	o	o	o		Write Multiple	x	o	o
Security Disable Password	x	o	x		Write Multiple Ext	x	o	o
Security Erase Prepare	o	o	x		Write Sector(s)	x	o	o
Security Erase Unit	o	o	x		Write Sector(s) Ext	x	o	o
Security Freeze Lock	x	o	o					

o - executable x - command aborted

10.9 Host Protected Area Feature

Host Protected Area Feature provides a protected area which cannot be accessed via conventional methods. This protected area is used to contain critical system data such as BIOS or system management information. The contents of the main memory of the entire system may also be dumped into the protected area to resume after a system power off.

The following set of commands changes the LBA/CYL, which affects the Identify Device Information:

- Read Native Max ADDRESS ('F8'h)
- Set Max ADDRESS ('F9'h)

10.9.1 Example for operation (In LBA Mode)

The following example uses hypothetical values.

Capacity (native)	6,498,680,832 byte (6.4 GB)
Max LBA (native)	12,692,735 (0FFFFFh)
Required size for protected area	206,438,400 bytes
Required blocks for protected area	403,200 (062700h)
Customer usable device size	6,292,242,432 byte (6.2 GB)
Customer usable sector count	12,289,536 (BB8600h)
LBA range for protected area	BB8600h to C1ACFFh

1. *Shipping of drives from the drive manufacturer*

   When the drive is shipped from the manufacturer, the device has been tested to have a capacity of 6.4 GB besides flagged media defects not visible by the system.

2. *Preparation of drives by the system manufacturer*

Special utility software is required to define the size of the protected area and to store the data in it. The sequence is as follows:

i. Issue a Read Native Max ADDRESS command to get the real device maximum LBA. Returned value shows that native device maximum LBA is 12,692,735 (C1ACFFh) regardless of the current setting.

ii. Make the entire device accessible, including the protected area, by setting the device maximum LBA to 12,692,735 (C1ACFFh) via Set Max ADDRESS command. The option may be either nonvolatile or volatile.

iii. Test the sectors for protected area (LBA > = 12,289,536 (BB8600h)) if required.

iv. Write information data such as BIOS code within the protected area.

v. Change maximum LBA using Set Max ADDRESS command to 12,289,535 (BB85FFh) with nonvolatile option.

vi. From this point the protected area cannot be accessed until next Set Max ADDRESS command is issued. Since the device functions in the same manner as a 6.2 GB device, any BIOS, device driver, or application software will access the drive as if it were a 6.2 GB device.

3. *Conventional usage without system software support*

   Since the drive works as a 6.2 GB device, there is no special care required for normal use of this device.

4. *Advanced usage using protected area*

   The data in the protected area is accessed by the following steps.

   i. Issue Read Native Max ADDRESS command to get the real device maximum LBA. Returned value shows that native device maqximum LBA is 12,692,735 (C1ACFFh) regardless of the current setting.

   ii. Make entire device accessible, including the protected area, by setting device maximum LBA as 12,692,735 (C1ACFFh) via the Set Max ADDRESS command with the volatile option. By using this option, unexpected power removal or reset will prevent the protected area from remaining accessible.

   iii. Read information data from protected area.

   iv. Issue hard reset or POR to inhibit any access to the protected area.

10.9.2 Security extensions

- Set Max Set Password
- Set Max Lock
- Set Max Freeze Lock
- Set Max Unlock

The Set Max Set Password command allows the host to define the password to be used during the current power on cycle. The password does not persist over a power cycle but does persist over a hardware or software reset. This password is not related to the password used for the Security Mode Feature set. When the password is set the device is in the Set_Max_Unlocked mode. The Set Max Lock command allows the host to disable the Set Max commands (except set Max Unlock) until the next power cycle or the issuance and acceptance of the Set Max Unlock command. When this command is accepted, the device is in the Set_Max_Locked mode. The Set Max Unlock command changes the device from the Set_Max_Locked mode to the Set_Max_Unlocked mode. The Set Max Freeze Lock command allows the host to disable the Set Max commands (including Set Max UNLOCK) until the next power cycle. When this command is accepted, the device is in the Set_Max_Frozen mode.

The IDENTIFY DEVICE response word 83, bit 8 indicates that this extension is supported if set, and word 86, bit 8 indicates the Set Max security extension is enabled if set.

10.10 Seek overlap

HDS7225xxVLATx0 provides an accurate method for measuring seek time. The seek command is usually used to measure the device seek time by accumulating the execution time for a number of seek commands. With typical implementation of seek command this measurement must include the device and host command overhead. To eliminate this overhead the drive overlaps the seek command as described below.

The first seek command is completed before the actual seek operation is ended. Then the device can receive the next seek command from the host; however, the actual seek operation for the next seek command starts immediately after the actual seek operation for the first seek command is completed. In other words, the execution of two seek commands overlaps excluding the time required for the actual seek operation.

With this overlap the total elapsed time for a number of seek commands results in the total accumulated time for actual seek operation plus one pre- and post-overhead. When the number of seeks is large, only one overhead may be ignored.

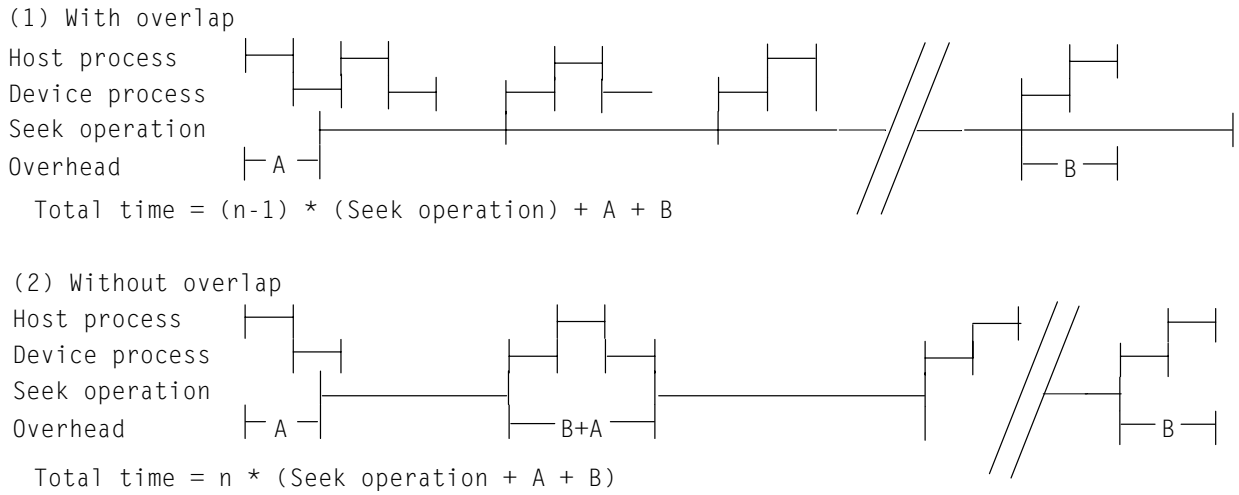


Figure 17 : Seek overlap

10.11 Write cache function

Write cache is a performance enhancement whereby the device reports the completion of the write command (Write Sectors, Write Multiple, and Write DMA) to the host as soon as the device has received all of the data into its buffer. The device assumes the responsibility for subsequently writing the data onto the disk.

- While writing data after completed acknowledgment of a write command, soft reset or hard reset does not affect its operation. However power off terminates the writing operation immediately and unwritten data is lost.
- The Soft reset, Standby (Immediate) command, and Flush Cache commands during the writing of the cached data are executed after the completion of writing to media. So the host system can confirm the completion of write cache operation by issuing a Soft reset, Standby (Immediate) command, or Flush Cache command to the device. before power off.

10.12 Reassign function

The Reassign function is used with read commands and write commands. The sectors of data for reassignment are prepared as the spare data sector.

This reassignment information is registered internally and the information is available right after completing the Reassign function. Also the information is used on the next power on reset or hard reset.

If the number of the spare sector reaches 0 sector, the Reassign function will be automatically disabled.

The spare sectors for reassignment are located at regular intervals from Cylinder 0. As a result of reassignment the physical location of logically sequenced sectors will be dispersed.

10.12.1 Auto Reassign function

The sectors which show some errors may be reallocated automatically when specific conditions are met. The spare tracks for reallocation are located at regular intervals from Cylinder 0. The conditions for auto- reallocation are described below.

10.12.1.1 Nonrecovered write errors

When a write operation cannot be completed after the Error Recovery Procedure (ERP) is fully carried out, the sector(s) are reallocated to the spare location. An error is reported to the host system only when the write cache is disabled and the auto reallocation has failed.

If the Write Cache function is ENABLED when the number of available spare sectors reaches 0 sector, both Auto Reassign function and Write Cache function are automatically disabled.

10.12.1.2 Nonrecovered read errors

When a read operation has failed after defined ERP is fully carried out, a hard error is reported to the host system. This location is registered internally as a candidate for reallocation. When a registered location is specified as a target of a write operation, a sequence of media verification is performed automatically. When the result of this verification meets the criteria, this sector is reallocated.

10.12.1.3 Recovered read errors

When a read operation for a sector has failed once and then has recovered at the specific ERP step, this sector of data is automatically reallocated. A media verification sequence may be run prior to the reallocation according to the predefined conditions.

10.13 Power-Up in Standby feature set

The Power-Up In Standby feature set allows devices to be powered-up into the Standby power management state to minimize inrush current at power-up and to allow the host to sequence the spin-up of devices.

This feature set will be enabled and disabled via the SET FEATURES command or the use of a jumper. When enabled by a jumper, the feature set shall not be disabled via the SET FEATURES command. The enabling of this feature set shall be persistent after power cycle.

A device needs a SET FEATURES subcommand to spin-up to active state when the device has powered up into Standby. The device remains in Standby until the SET FEATURES subcommand is received.

If power-up into Standby is enabled when an IDENTIFY DEVICE is received while the device is in Standby as a result of powering up into Standby, the device shall set word 0 bit 2 to one to indicate that the response is incomplete, only words 0 and 2 are correctly reported.

The IDENTIFY DEVICE information indicates the states as follows:

- identify device information is complete or incomplete
- this feature set is implemented
- this feature set is enabled or disabled
- the device needs the Set Features command to spin-up into active state

10.14 Advanced Power Management feature set (APM)

This feature allows the host to select an advanced power management level. The advanced power management level is a scale from the lowest power consumption setting of 01h to the maximum performance level of FEh. Device performance may increase with increasing advanced power management levels. Device power consumption may increase with increasing advanced power management levels. The advanced power management levels contain discrete bands described in the section of SET FEATURES command in detail. This feature set uses the following functions:

- A SET FEATURES subcommand to enable Advanced Power Management
- A SET FEATURES subcommand to disable Advanced Power Management

Advanced Power Management, Automatic Acoustic Management, and the Standby timer setting are independent functions. The device shall enter Standby mode if any of the following are true:

1. The Standby timer has been set and times out
2. Automatic Power Management is enabled and the associated algorithm indicates that the Standby mode should be entered to save power
3. Automatic Acoustic Management is enabled and the associated algorithm indicates that the Standby mode should be entered to reduce acoustical emanations

The IDENTIFY DEVICE response word 83, bit 3 indicates that Advanced Power Management feature is supported if set. Word 86, bit 3 indicates that Advanced Power Management is enabled if set. Word 91, bits 7-0 contains the current Advanced Power Management level if it is enabled.

10.15 Automatic Acoustic Management feature set (AAM)

This feature set allows the host to select an acoustic management level. The acoustic management level may range from the lowest acoustic emanation setting of 01h to the maximum performance level of FEh. Device performance and acoustic emanation may increase with increasing acoustic management levels. The acoustic management levels may contain discrete bands. Automatic Acoustic Management levels 80h and higher do not permit the device to enter Standby mode as a result of the Automatic Acoustic Management algorithm. The Automatic Acoustic Management feature set uses the following functions:

1. A SET FEATURES subcommand to enable Automatic Acoustic Management
2. A SET FEATURES subcommand to disable Automatic Acoustic Management

Advanced Power Management, Automatic Acoustic Management, and the Standby timer setting are independent functions. The device shall enter Standby mode if any of the following are true:

1. The Standby timer has been set and times out.
2. Automatic Power Management is enabled and the associated algorithm indicates that the Standby mode should be entered to save power.
3. Automatic Acoustic Management is enabled and the associated algorithm indicates that the Standby mode should be entered to reduce acoustical emanations.

The IDENTIFY DEVICE response word 83, bit 9 indicates that Automatic Acoustic Management feature is supported if set. Word 86, bit 9 indicates that Automatic Acoustic Management is enabled if set. Word 94, bits 7-0s contains the current Automatic Acoustic Management level if Automatic Acoustic Management is enabled, and bits 8-15 contain the Vendor's recommended AAM level.

10.16 Address Offset Feature

Computer systems perform initial code loading (booting) by reading from a predefined address on a drive. To allow an alternate bootable operating system to exist in a system reserved area on a drive, this feature provides a Set Features function to temporarily offset the drive address space. The offset address space wraps around so that the entire drive address space remains addressable in offset mode. Max LBA in offset mode is set to the end of the system reserved area to protect the data in the user area when operating in offset mode. The Max LBA can be changed by a Set Max Address command to access the user area. If the native MAX LBA is set, the whole user area can be accessed. But any commands which access sectors across the original native maximum LBA are rejected with error, even if this protection is removed by an Set Max Address command.

10.16.1 Enable/Disable Address Offset Mode

Subcommand code 09h Enable Address Offset Mode offsets address Cylinder 0, Head 0, Sector 1, LBA 0, to the start of the nonvolatile protected area established using the Set Max Address command. The offset condition is cleared by Subcommand 89h Disable Address Offset Mode, Hardware reset or Power on Reset. If Reverting to Power on Defaults has been enabled by Set Features command, it is cleared by Soft reset as well. Upon entering offset mode the capacity of the drive returned in the Identify Device data is the size of the former protected area. A subsequent Set Max Address command with the address returned by the Read Max Address command allows access to the entire drive. Addresses wrap so the entire drive remains addressable.

If a nonvolatile protected area has not been established before the device receives a Set Features Enable Address Offset Mode command, the command fails with Abort error status.

Disable Address Offset Feature removes the address offset and sets the size of the drive reported by the Identify Device command back to the size specified in the last nonvolatile Set Max Address command.

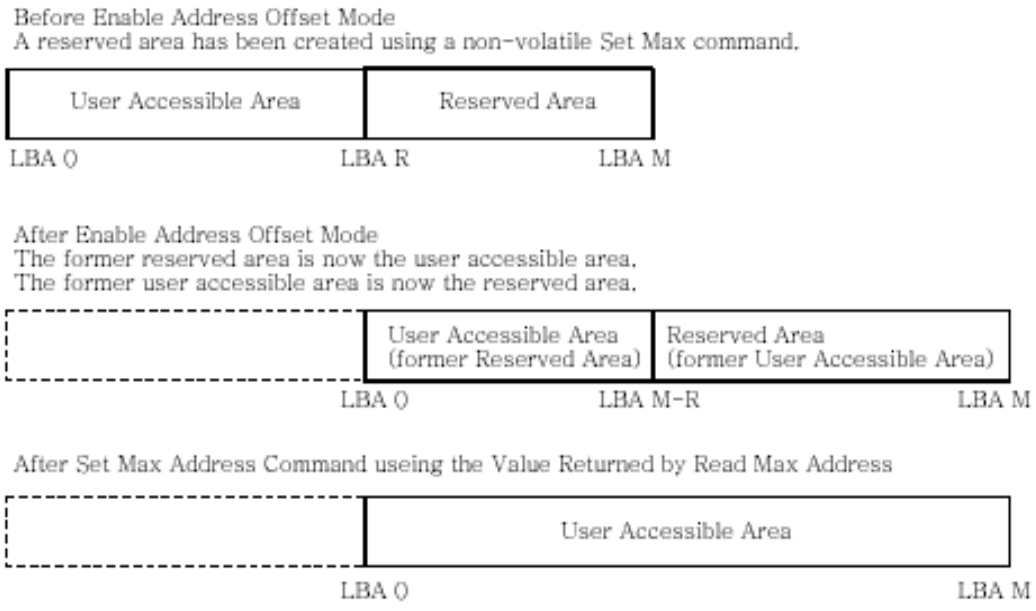


Figure 18 : Device address map before and after Set Feature

10.16.2 Identify Device Data

Identify Device data, word 83, bit 7 indicates the device supports the Address Offset Feature. Identify Device data, word 86, bit 7 indicates the device is in Address Offset mode.

10.16.3 Exceptions in Address Offset Mode

Any commands which access sectors across the original native maximum LBA are rejected with error, even if the access protection is removed by a Set Max Address command.

If the sectors for Read Look Ahead operation include the original native maximum LBA, Read Look Ahead operation is not carried out, even if it is enabled by the Set Feature command.

10.17 48-bit Address Feature Set

The 48-bit Address feature set allows devices with capacities up to 281,474,976,710,655 sectors. This allows device capacity up to 144,115,188,075,855,360 bytes. In addition, the number of sectors that may be transferred by a single command are increased by increasing the allowable sector count to 16 bits.

Commands unique to the 48-bit Address feature set are

- Flush Cache Ext
- Read DMA Ext
- Read DMA Queued Ext
- Read Multiple Ext
- Read Native Max Address Ext
- Read Sector(s) Ext
- Read Verify Sector(s) Ext
- Set Max Address Ext
- Write DMA Ext
- Write DMA Queued Ext
- Write Multiple Ext
- Write Sector(s) Ext

The 48-bit Address feature set operates in LBA addressing only. Devices also implement commands using 28-bit addressing, and 28-bit and 48-bit commands may be intermixed.

In a device, the Features, the Sector Count, the Sector Number, the Cylinder High, and the Cylinder Low registers are a two-byte-deep FIFO. Each time one of these registers is written, the new content written is placed into the "most recently written" location and the previous content is moved to "previous content" location.

The host may read the "previous content" of the Features, the Sector Count, the Sector Number, the Cylinder High, and the Cylinder Low registers by first setting the High Order Bit (HOB, bit 7) of the Device control register to one and then reading the desired register. If HOB in the Device Control register is cleared to zero, the host reads the "most recently written" content when the register is read. A write to any Command Block register shall cause the device to clear the HOB bit to zero in the Device Control register. The "most recently written" content always gets written by a register write regardless of the state of HOB in the Device Control register.

Support of the 48-bit Address feature set is indicated in the Identify Device response bit 10 word 83. In addition, the maximum user LBA address accessible by 48-bit addressable commands is contained in Identify Device response words 100 through 103.

When the 48-bit Address feature set is implemented, the native maximum address is the value returned by a Read Native Max Address Ext command. If the native maximum address is equal to or less than 268,435,455, a Read Native Max Address shall return the native maximum address. If the native maximum address is greater than 268,435,455, a Read Native Max Address shall return a value of 268,435,455.

11.0 Command protocol

The commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host must first check to see if BSY = 1, and should proceed no further unless and until BSY = 0. For all commands, the host must also wait for RDY = 1 before proceeding.

A device must maintain either BSY = 1 or DRQ = 1 at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from 1 to 0 during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while BSY = 1 or DRQ = 1 is unpredictable and may result in data corruption. A command should only be interrupted by a reset at times when the host thinks there may be a problem, such as a device that is no longer responding.

Interrupts are cleared when the host reads the Status Register, issues a reset, or writes to the Command Register.

See Section 13.0, “Time-out values” on page 221 for the device time-out values.

11.1 PIO Data In commands

The following are Data In commands:

- Device Configuration Identity
- Identify Device
- Read Buffer
- Read Log Ext
- Read Long
- Read Multiple
- Read Multiple Ext
- Read Sector(s)
- Read Sector(s) Ext
- S.M.A.R.T. Read Attribute Values
- S.M.A.R.T. Read Attribute Thresholds
- S.M.A.R.T. Read log sector

Execution includes the transfer of one or more 512 byte (> 512 bytes on Read Long) sectors of data from the device to the host.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. For each sector (or block) of data to be transferred:
   a. The device sets BSY = 1 and prepares for data transfer.
   b. When a sector (or block) of data is available for transfer to the host, the device sets BSY = 0, sets DRQ = 1, and interrupts the host.
   c. In response to the interrupt the host reads the Status Register.
   d. The device clears the interrupt in response to the Status Register being read.

e. The host reads one sector (or block) of data via the Data Register.

f. The device sets DRQ = 0 after the sector (or block) has been transferred to the host.

4. For the Read Long command:
   a. The device sets BSY = 1 and prepares for data transfer.
   b. When the sector of data is available for transfer to the host, the device sets BSY = 0 and DRQ=1 and interrupts the host.
   c. In response to the interrupt, the host reads the Status Register.
   d. The device clears the interrupt in response to the Status Register being read.
   e. The host reads the sector of data including ECC bytes via the Data Register.
   f. The device sets DRQ = 0 after the sector has been transferred to the host.

The Read Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

Note that the status data for a sector of data is available in the Status Register **before** the sector is transferred to the host.

If the device detects an invalid parameter, then it will abort the command by setting BSY = 0, ERR = 1, ABT = 1, and interrupting the host.

If an error occurs, the device will set BSY = 0, ERR = 1, and DRQ = 1. The device will then store the error status in the Error Register and interrupt the host. The registers will contain the location of the sector in error. The error location will be reported using CHS mode or LBA mode. The mode is decided by the mode select bit (bit 6) of the Device/Head register upon issuing the command.

If an Uncorrectable Data Error (UNC = 1) occurs, the defective data will be transferred from the media to the sector buffer and will be available for transfer to the host at the host's option. In case of a Read Multiple command, the host should complete transfer of the block which includes the error from the sector buffer and terminate whatever type of error that occurred.

All data transfers to the host through the Data Register are 16 bits except for the ECC bytes which are 8 bits.

11.2 PIO Data Out Commands

The following are Data Out commands:

- Device Configuration SET
- Format Track
- Security Disable Password
- Security Erase Unit
- Security Set Password
- Security Unlock
- Set Max Set Password
- Set Max Unlock
- S.M.A.R.T. Write log sector
- Write Buffer
- Write Log Ext
- Write Long
- Write Multiple

- Write Multiple Ext
- Write Sector(s)
- Write Sector(s) Ext

Execution includes the transfer of one or more 512 byte (> 512 bytes on Write Long) sectors of data from the host to the device.

1. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
2. The host writes the command code to the Command Register.
3. The device sets BSY = 1.
4. For each sector (or block) of data to be transferred:
   a. The devics BSY = 0 and DRQ = 1 when it is ready to receive a sector (or block).
   b. The host writes one sector (or block) of data via the Data Register.
   c. The device sets BSY = 1 after it has received the sector (or block).
   d. When the device has finished processing the sector (or block), it sets BSY = 0 and interrupts the host.
   e. In response to the interrupt, the host reads the Status Register.
   f. The device clears the interrupt in response to the Status Register being read.
5. For the Write Long command:
   a. The device sets BSY = 0 and DRQ = 1 when it is ready to receive a sector.
   b. The host writes one sector of data including ECC bytes via the Data Register.
   c. The device sets BSY = 1 after it has received the sector.
   d. After processing the sector of data, the device sets BSY = 0 and interrupts the host.
   e. In response to the interrupt the host reads the Status Register.
   f. The device clears the interrupt in response to the Status Register being read.

The Write Multiple command transfers one block of data for each interrupt. The other commands transfer one sector of data for each interrupt.

If the device detects an invalid parameter, it will abort the command by setting BSY = 0, ERR = 1, ABT = 1, and interrupting the host.

If an uncorrectable error occurs, the device will set BSY = 0 and ERR = 1, store the error status in the Error Register, and interrupt the host. The registers will contain the location of the sector in error. The errored location will be reported with CHS mode or LBA mode. The mode is decided by the mode select bit (bit 6) of the Device/Head register on issuing the command.

All data transfers to the device through the Data Register are 16 bits except for the ECC bytes which are 8 bits.

11.3 Non-data commands

The following are Non-data commands:

- Check Power Mode
- Device Configuration FREEZE LOCK
- Device Configuration RESTORE
- Execute Device Diagnostic
- Flush Cache
- Flush Cache Ext
- Idle
- Idle Immediate
- Initialize Device Parameters
- NOP
- Read Native Max ADDRESS
- Read Native Max ADDRESS Ext
- Read Verify Sector(s)
- Read Verify Sector(s) Ext
- Recalibrate
- Security Erase Prepare
- Security Freeze Lock
- Seek
- Set Features
- Set Max ADDRESS
- Set Max ADDRESS Ext
- Set Max LOCK
- Set Max FREEZE LOCK
- Set Multiple Mode
- Sleep
- S.M.A.R.T. Disable Operations
- S.M.A.R.T. Enable/Disable Attribute Autosave
- S.M.A.R.T. Enable/Disable Automatic Off Line
- S.M.A.R.T. Enable Operations
- S.M.A.R.T. Execute Off-line Data Collection
- S.M.A.R.T. Return Status
- S.M.A.R.T. Save Attribute Values
- Standby
- Standby Immediate

Execution of these commands involves no data transfer:

a. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head Registers.
b. The host writes the command code to the Command Register.
c. The device sets BSY = 1.
d. When the device has finished processing the command, it sets BSY = 0 and interrupts the host.
e. In response to the interrupt the host reads the Status Register.
f. The device clears the interrupt in response to the Status Register being read

11.4 DMA commands

The following are DMA commands:

- Read DMA
- Read DMA Ext
- Write DMA
- Write DMA

Data transfers using DMA commands differ in two ways from PIO transfers:

- Data transfers are performed using the Slave DMA channel
- No intermediate sector interrupts are issued on multisector commands.

Initiation of the DMA transfer commands is identical to the Read Sector(s) or Write Sector(s) commands with one exception: the host initializes the Slave DMA channel prior to issuing the command.

The interrupt handler for DMA transfers differs in two ways:

- No intermediate sector interrupts are issued on multisector commands.
- The host resets the DMA channel prior to reading status from the device

The DMA protocol allows high performance multitasking operating systems to eliminate processor overhead associated with PIO transfers.

1. The host initializes the Slave DMA channel.
2. The host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head registers.
3. The host writes command code to the Command Register.
4. The device sets DMARQ when it is ready to transfer any part of the data.
5. The host transfers the data using the DMA transfer protocol currently in effect.
6. When all of the data has been transferred, the device generates an interrupt to the host.
7. The host resets the Slave DMA channel.
8. The host reads the Status Register and, optionally, the Error Register.

11.5 DMA queued commands

DMA queued commands are

- Read DMA Queued
- Read DMA Queued Ext
- Service
- Write DMA Queued
- Write DMA Queued Ext

1. Command Issue
    a. the host writes any required parameters to the Features, Sector Count, Sector Number, Cylinder, and Device/Head registers.
    b. the host writes command code to the Command Register.
    c. the device sets BSY.
    d. the device clears or sets REL.
    e. the device clears BDY.

2. Data Transfer and Command Completion. If the device is ready for data transfer (REL is cleared),
    a. the host transfers the data for the command identified by the Tag number using tghe DMA transfer protocol currently in effect.
    b. the device generates an interrupt to the host when all of the data has been transferred.
    c. the host may issue another command or wait for service request from the device.

3. Bus release. If the device is not ready for data ttransfer (REL is sent),
    a. the device generates an interrupt if release interrupt is enabled.
    b. the host may issue another command or wait for service request from the device.

12.0 Command descriptions

The table below shows the commands that are supported by the device. Table 50: “Command Set (subcommand)” on page 107 shows the subcommands that are supported by each command or feature.

Table 48: Command Set (1 of 2)

Protocol	Command	Code (Hex)	Binary Code Bit 7 6 5 4 3 2 1 0
3	Check Power Mode	E5	1 1 1 0 0 1 0 1
3	Check Power Mode*	98	1 0 0 1 1 0 0 0
3	Device Configuration RESTORE	B1	1 0 1 1 0 0 0 1
3	Device Configuration FREEZE LOCK	B1	1 0 1 1 0 0 0 1
1	Device Configuration IDENTIFY	B1	1 0 1 1 0 0 0 1
2	Device Configuration SET	B1	1 0 1 1 0 0 0 1
3	Execute Device Diagnostic	90	1 0 0 1 0 0 0 0
3	Flush Cache	E7	1 1 1 0 0 1 1 1
3	Flush Cache Ext	EA	1 1 1 0 1 0 1 0
2	Format Track	50	0 1 0 1 0 0 0 0
3	Format Unit	E7	1 1 1 1 0 1 1 1
1	Identify Device	EC	1 1 1 0 1 1 0 0
3	Idle	E3	1 1 1 0 0 0 1 1
3	Idle*	97	1 0 0 1 0 1 1 1
3	Idle Immediate	E1	1 1 1 0 0 0 0 1
3	Idle Immediate*	95	1 0 0 1 0 1 0 1
3	Initialize Device Parameters	91	1 0 0 1 0 0 0 1
3	NOP	00	0 0 0 0 0 0 0 0
1	Read Buffer	E4	1 1 1 0 0 1 0 0
4	Read DMA	C8	1 1 0 0 1 0 0 0
4	Read DMA	C9	1 1 0 0 1 0 0 1
4	Read DMA Ext	25	0 0 1 0 0 1 0 1
5	Read DMA Queued	C7	1 1 0 0 0 1 1 1
5	Read DMA Queued Ext	26	0 0 1 0 0 1 1 0
1	Read Long	22	0 0 1 0 0 0 1 0
1	Read Long	23	0 0 1 0 0 0 1 1
1	Read Log Ext	2F	0 0 1 0 1 1 1 1
1	Read Multiple	C4	1 1 0 0 0 1 0 0
1	Read Multiple Ext	29	0 0 1 0 1 0 0 1
3	Read Native Max ADDRESS	F8	1 1 1 1 1 0 0 0
3	Read Native Max ADDRESS Ext	27	0 0 1 0 0 1 1 1
1	Read Sector(s)	20	0 0 1 0 0 0 0 0
1	Read Sector(s)	21	0 0 1 0 0 0 0 1
1	Read Sector(s) Ext	24	0 0 1 0 0 1 0 0
3	Read Verify Sector(s)	40	0 1 0 0 0 0 0 0
3	Read Verify Sector(s)	41	0 1 0 0 0 0 0 1
3	Read Verify Sector(s) Ext	42	0 0 0 1 - - - -
3	Recalibrate	1x	0 0 0 1 - - - -
2	Security Disable Password	F6	1 1 1 1 1 0 1 0
3	Security Erase Prepare	F3	1 1 1 1 0 0 1 1
2	Security Erase Unit	F4	1 1 1 1 0 1 0 0

Table 49: Command Set (2 of 2)

Protocol	Command	Code (Hex)	Binary Code Bit							
			7	6	5	4	3	2	1	0
3	Security Freeze Lock	F5	1	1	1	1	0	1	0	1
2	Security Set Password	F1	1	1	1	1	0	0	0	1
2	Security Unlock	F2	1	1	1	1	0	0	1	0
3	Seek	7x	0	1	1	1	-	-	-	-
5	Service	A2	1	0	1	0	0	0	1	0
3	Set Features	EF	1	1	1	0	1	1	1	1
3	Set Max ADDRESS	F9	1	1	1	1	1	0	0	1
3	Set Max ADDRESS Ext	37	0	0	1	1	0	1	1	1
3	Set Multiple Mode	C6	1	1	0	0	0	1	1	0
3	Sleep	E6	1	1	1	0	0	1	1	0
3	Sleep*	99	1	0	0	1	1	0	0	1
3	S.M.A.R.T. Disable Operations	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Enable/Disable Attribute Auto save	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Enable/Disable Automatic Off-line	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Enable Operations	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Execute Off-line Data Collection	B0	1	0	1	1	0	0	0	0
1	S.M.A.R.T. Read Attribute Values	B0	1	0	1	1	0	0	0	0
1	S.M.A.R.T. Read Attribute Thresholds	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Return Status	B0	1	0	1	1	0	0	0	0
3	S.M.A.R.T. Save Attribute Values	B0	1	0	1	1	0	0	0	0
2	S.M.A.R.T. Write Log Sector	B0	1	0	1	1	0	0	0	0
3	Standby	E2	1	1	1	0	0	0	1	0
3	Standby*	96	1	0	0	1	0	1	1	0
3	Standby Immediate	E0	1	1	1	0	0	0	0	0
3	Standby Immediate*	94	1	0	0	1	0	1	0	0
2	Write Buffer	E8	1	1	1	0	1	0	0	0
4	Write DMA	CA	1	1	0	0	1	0	1	0
4	Write DMA	CB	1	1	0	0	1	0	1	1
4	Write DMA Ext	35	0	0	1	1	0	1	0	1
5	Write DMA Queued	CC	1	1	0	0	1	1	0	0
5	Write DMA Queued Ext	36	0	0	1	1	0	1	1	0
2	Write Log Ext	3F	0	0	1	1	1	1	1	1
2	Write Long	32	0	0	1	1	0	0	1	0
2	Write Long	33	0	0	1	1	0	0	1	1
2	Write Multiple	C5	1	1	0	0	0	1	0	1
2	Write Multiple Ext	39	0	0	1	1	1	0	0	1
2	Write Sector(s)	30	0	0	1	1	0	0	0	0
2	Write Sector(s)	31	0	0	1	1	0	0	0	1
2	Write Sector(s)Ext	34	0	0	1	1	0	1	0	0

Commands marked * are alternate command codes for previously defined commands

Protocol: 1 : PIO data IN command

2 : PIO data OUT command
3 : Non data command
4 : DMA command
5 :

Table 50: Command Set (subcommand)

Command (Subcommand)	Command Code (Hex)	Feature Register (Hex)
S.M.A.R.T. Function		
S.M.A.R.T. Read Attribute Values	B0	D0
S.M.A.R.T. Read Attribute Thresholds	B0	D1
S.M.A.R.T. Enable/Disable Attribute Autosave	B0	D2
S.M.A.R.T. Save Attribute Values	B0	D3
S.M.A.R.T. Execute Off-line Immediate	B0	D4
S.M.A.R.T. Read Log	B0	D5
S.M.A.R.T. Write Log	B0	D6
S.M.A.R.T. Enable Operations	B0	D8
S.M.A.R.T. Disable Operations	B0	D9
S.M.A.R.T. Return Status	B0	DA
S.M.A.R.T. Enable/Disable Automatic Off-line	B0	DB
Set Features		
Enable Write Cache	EF	02
Set Transfer mode	EF	03
Enable Advanced Power Management	EF	05
Enable Power-up in Standby Feature Set	EF	06
Power-up in Standby Feature Set Device Spin-up	EF	07
Enable Address Offset mode	EF	09
Enable Automatic Acoustic Management	EF	42
52 bytes of ECC apply on Read/Write Long	EF	44
Disable read look-ahead feature	EF	55
Enable release interrupt	EF	5D
Disable reverting to power on defaults	EF	66
Disable write cache	EF	82
Disable Advanced Power Management	EF	85
Disable Power-up in Standby Feature Set	EF	86
Disable Address Offset mode	EF	89
Enable read look-ahead feature	EF	AA
4 bytes of ECC apply on Read/Write Long	EF	BB
Disable Automatic Acoustic Management	EF	C2
Enable reverting to power on defaults	EF	CC
Disable release interrupt	EF	DD

The following symbols are used in the command descriptions.

Output registers

0	This indicates that the bit must be set to 0.
1	This indicates that the bit must be set to 1.
D	The device number bit. Indicates that the device number bit of the Device/Head Register should be specified. Zero selects the master device and one selects the slave device.
H	Head number. This indicates that the head number part of the Device/Head Register is an output parameter and should be specified.
L	LBA mode. This indicates the addressing mode. Zero specifies CHS mode and one specifies LBA addressing mode.
R	Retry. Original meaning is already obsolete, there is no difference between 0 and 1. (Using 0 is recommended for future compatibility.)
B	Option Bit. This indicates that the Option Bit of the Sector Count Register be specified. (This bit is used by Set Max ADDRESS command.)
V	Valid. This indicates that the bit is part of an output parameter and should be specified.
x	This indicates that the hex character is not used.
-	This indicates that the bit is not used.

Input registers

0	This indicates that the bit is always set to 0.
1	This indicates that the bit is always set to 1.
H	Head number. This indicates that the head number part of the Device/Head Register is an input parameter and will be set by the device.
V	Valid. This indicates that the bit is part of an input parameter and will be set by the device to 0 or 1.
N	Not recommended condition for start up. Indicates that the condition of the device is not recommended for start up.
-	This indicates that the bit is not part of an input parameter. Symbols are used in the command descriptions:

The command descriptions show the contents of the Status and Error Registers after the device has completed processing the command and has interrupted the host.

12.1 Check Power Mode (E5h/98h)

Table 51: Check Power Mode command (E5h/98h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	V V V V V V V V
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 0 1 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Check Power Mode command will report whether the device is spun up and the media is available for immediate access.

Input parameters from the device

Sector Count This indicates the power mode code. The command returns FFh in the Sector Count Register if the spindle motor is at speed and the device is not in Standby or Sleep mode. Otherwise, the Sector Count Register is set to 0.

12.2 Device Configuration Overlay (B1h)

Table 52: Check Power Mode Command (E5h/98h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	1 0 1 0 V V V V		Error	see below
Sector Count	- - - - - - - -		Sector Count	V V V V V V V V
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	V V V V V V V V
Cylinder High	- - - - - - - -		Cylinder High	V V V V V V V V
Device/Head	- - - D - - - -		Device/Head	- - - - - - - -
Command	1 0 1 1 0 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		V	V	0	-	V	-	-	V

Individual Device Configuration Overlay feature set commands are identified by the value placed in the Features register. The table below shows these Features register values.

Table 53: Device Configuration Overlay Features register values

Value	Command
C0h	DEVICE CONFIGURATION RESTORE
C1h	DEVICE CONFIGURATION FREEZE LOCK
C2h	DEVICE CONFIGURATION IDENTIFY
C3h	DEVICE CONFIGURATION SET
other	Reserved

12.2.1 DEVICE CONFIGURATION RESTORE

The DEVICE CONFIGURATION RESTORE command disables any setting previously made by a DEVICE CONFIGURATION SET command and returns the content of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command response to the original settings as indicated by the data returned from the execution of a DEVICE CONFIGURATION IDENTIFY command.

12.2.2 DEVICE CONFIGURATION FREEZE LOCK (subcommand C1h)

The DEVICE CONFIGURATION FREEZE LOCK command prevents accidental modification of the Device Configuration Overlay settings. After successful execution of a DEVICE CONFIGURATION FREEZE LOCK command, all DEVICE CONFIGURATION SET, DEVICE CONFIGURATION FREEZE LOCK, DEVICE CONFIGURATION IDENTIFY, and DEVICE CONFIGURATION RESTORE commands are aborted by the device. The DEVICE CONFIGURATION FREEZE LOCK condition shall be cleared by a power-down. The DEVICE CONFIGURATION FREEZE LOCK condition shall not be cleared by hardware or software reset.

12.2.3 DEVICE CONFIGURATION IDENTIFY (subcommand C2h)

The DEVICE CONFIGURATION IDENTIFY command returns a 512 byte data structure via PIO data-in transfer. The content of this data structure indicates the selectable commands, modes, and feature sets that the device is capable of supporting. If a DEVICE CONFIGURATION SET command has been issued reducing the capabilities, the response to an IDENTIFY DEVICE or IDENTIFY PACKET DEVICE command will reflect the reduced set of capabilities, while the DEVICE CONFIGURATION IDENTIFY command will reflect the entire set of selectable capabilities.

The format of the Device Configuration Overlay data structure is shown in Table 54: "Device Configuration Overlay Data structure" on page 112.

12.2.4 DEVICE CONFIGURATION SET (subcommand C3h)

The DEVICE CONFIGURATION SET command allows a device manufacturer or a personal computer system manufacturer to reduce the set of optional commands, modes, or feature sets supported by a device as indicated by a DEVICE CONFIGURATION IDENTIFY command. The DEVICE CONFIGURATION SET command transfers an overlay that modifies some of the bits set in words 63, 82, 83, 84, and 88 of the IDENTIFY DEVICE command response. When the bits in these words are cleared, the device no longer support the indicated command, mode, or feature set. If a bit is set in the overlay transmitted by the device that is not set in the overlay received from a DEVICE CONFIGURATION IDENTIFY command, no action is taken for that bit.

The format of the overlay transmitted by the device is described in the table in Table 54: "Device Configuration Overlay Data structure" on page 112. The restrictions on changing these bits is described in the text following that table. If any of the bit modification restrictions described are violated or any setting is changed with DEVICE CONFIGURATION SET command, the device shall return command aborted. At that case, error reason code is returned to sector count register, invalid word location is returned to cylinder high register, and invalid bit location is returned to cylinder low register. The Definition of error information is shown in Table 55: "DCO error information definition" on page 113.

ERROR INFORMATION EXAMPLE 1:

If a user attempts to change maximum LBA address (DC SET or DC RESTORE) after establishing a protected area with SET MAX address, the device will abort that command and returns error reason code as below.

```
Cylinder high  :   03h = word 3 is invalid
Cylinder low   :   00h this register is not assigned in this case
Sector count   :   06h = Protected area is now established
```

ERROR INFORMATION EXAMPLE 2:

If the user attempts to disable that feature when the device is enabled and the Security feature is set, the device will abort that command and returns an error reason code as below.

```
Cylinder high  :   07h = word 7 is invalid
Cylinder low   :   08h = bit 3 is invalid
Sector count   :   04h = Security feature set is now enabled
```

Table 54: Device Configuration Overlay Data structure

Word	Content	
0	0001h	Data Structure revision
1	Multiword DMA modes supported	
	15-3	Reserved
	2	1 = Multiword DMA mode 2 and below are supported
	1	1 = Multiword DMA mode 1 and below are supported
	0	1 = Multiword DMA mode 0 is supported
2	Ultra DMA modes supported	
	15-6	Reserved
	5	1 = Ultra DMA mode 5 and below are supported
	4	1 = Ultra DMA mode 4 and below are supported
	3	1 = Ultra DMA mode 3 and below are supported
	2	1 = Ultra DMA mode 2 and below are supported
	1	1 = Ultra DMA mode 1 and below are supported
	0	1 = Ultra DMA mode 0 is supported
3-6	Maximum LBA address	
7	Command set/feature set supported	
	15-9	Reserved
	8	1 = 48-bit addressing feature set supported
	7	1 = Host Protected Area feature set supported
	6	1 = Automatic acoustic management supported
	5	1 = Read/Write DMA Queued commands supported
	4	1 = Power-up in Standby feature set supported
	3	1 = Security feature set supported
	2	1 = SMART error log supported
	1	1 = SMART self-test supported
	0	1 = SMART feature set supported
8-254	Reserved	
255	Integrity word (see note below)	
	15-8	Checksum
	7-0	Signature (A5h)

Note: Bits 7–0 of this word contain the value A5h. Bits 15–8 of this word contain the data structure checksum. The data structure checksum is the two's complement of the sum of all byte in words 0 through 254 and the byte consisting of bits 7–0 of word 255. Each byte is added with unsigned arithmetic and overflow is ignored. The sum of all bytes is zero when the checksum is correct.

Table 55: DCO error information definition

Cylinder high	invalid word location	
Cylinder low	invalid bit location (bits 7:0)	
Sector Number	Invalid bit location (bits 15:8)	
Sector count	*error reason code*	*description*
	01h	DCO feature is frozen
	02h	Device is now Security Locked mode
	03h	Device's feature is already modified with DCO
	04h	User attempt to disable any feature enabled
	05h	Device is now SET MAX Locked or Frozen mode
	06h	Protected area is now established
	07h	DCO is not supported
	08h	Subcommand code is invalid
	FFh	other reason

12.3 Execute Device Diagnostic (90h)

Table 56: Execute Device Diagnostic command (90h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 - - - - -		Device/Head	- - - - - - - -
Command	1 0 0 1 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	V	V	V	V	V	V		0	V	0	-	-	0	-	0

The Execute Device Diagnostic command performs the internal diagnostic tests implemented by the device. The results of the test are stored in the Error Register.

The normal Error Register bit definitions do not apply to this command. Instead, the register contains a diagnostic code. See Table 43: “Default Register Values” on page 74 for the definition.

12.4 Flush Cache (E7h)

Table 57: Flush Cache command (E7h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 0 1 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

This command causes the device to complete writing data from its cache.

The device returns good status after data in the write cache is written to the disk media.

12.5 Flush Cache Ext (EAh)

Table 58: Flush Cache Ext Command (EAh)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	- - - - - - - -		Sector Count	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Sector Number	Current	- - - - - - - -		Sector Number	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Cylinder Low	Current	- - - - - - - -		Cylinder Low	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Cylinder High	Current	- - - - - - - -		Cylinder High	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Device/Head		- - - D - - - -		Device/Head		- - - - - - - -
Command		1 1 1 0 1 0 1 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

This command causes the device to complete writing data from its cache.

The device returns good status after data in the write cache is written to disk media.

12.6 Format Track (50h)

Table 59: Format Track command (50h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 1 0 1 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Format Track command formats a single logical track on the device. Each good sector of data on the track will be initialized to zero with the write operation. At this time, the read operation does not verify the correct initialization of the data sector. Any data previously stored on the track will be lost.

The host may transfer a sector of data containing a format table to the device. But the device ignores the format table and writes zero to all sectors on the track regardless of the descriptors.

Since device performance is optimal at 1:1 interleave and the device uses relative block addressing internally, the device will always format a track in the same way no matter what sector numbering is specified in the format table.

Output parameters to the device

Sector Number In LBA mode this register specifies that LBA address bits 0–7 are to be formatted. (L=1).

Cylinder High/Low This indicates the cylinder number of the track to be formatted. (L = 0)

In LBA mode this register specifies that LBA address bits 8–15 (Low) and bits 16–23 (High) are to be formatted. (L = 1)

H This indicates the head number of the track to be formatted (L = 0). In LBA mode this register specifies that LBA address bits 24–27 are to be formatted. (L= 1)

Input parameters from the device

Sector Number In LBA mode this register specifies the current LBA address bits as 0–7 (L = 1).

Cylinder High/Low In LBA mode this register specifies the current LBA address bits as 8–15 (Low) and bits 16–23 (High).

H In LBA mode this register specifies the current LBA address bits as 24–27 (L=1).

Error The Error Register. An Abort error (ABT=1) will be returned when LBA is out of range

In LBA mode this command formats a single logical track including the specified BLA.

12.7 Format Unit (F7h)

Table 60: Format Unit command (F7h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	0 0 0 1 0 0 0 1		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 L 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 1 0 1 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	V		0	V	V	V	0	0	-	V

The Format Unit command initializes all user data sectors after merging the reassigned sector location into the defect information of the device and clearing the reassign information. Both new reassign information and new defect information are available immediately after the completion of this command and are also used on the next power-on reset or hard reset. This command erases both previous information data from the device.

Note that the Format Unit command initializes from LBA 0 to Native MAX LBA regardless of the setting by the Initialize Device Parameter (91h) command or the Set Max Address (F9h) command, so that the protected area defined by these commands is also initialized.

The Security Erase Prepare (F3h) command should be completed immediately prior to the Format Unit command. If the device receives a Format Unit command without a prior Security Erase Prepare command, the device aborts the Format Unit command.

All values in Feature register are reserved and any values other than 11h should not be put into Feature register.

This command does not request a data transfer.

Command execution time depends on drive capacity.

To determine the command time-out value, refer to Word 89 of Identify Device data.

12.8 Identify Device (ECh)

Table 61: Identify Device command (ECh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 1 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Identify Device command requests the device to transfer configuration information to the host. The device will transfer a sector to the host containing the information in Table 62 beginning on page 120.

Table 62: Identify device information (Part 1 of 7)

An asterisk (*) in next to the Content field indicates the use of those parameters that are vendor specific.

Word	Content		Description	
00	045AH or 045Eh		*drive classi-fication*	*bit assignments*
			15(=0)	1=ATAPI device, 0=ATA device
			14 - 8	retired
			7(=0)	1=removable cartridge drive
			6(=1)	1=fixed drive
			5 - 3	retired
			2(=0)	1=soft sectored
			1	retired
			0(=0)	Reserved
01	XXXXH		Number of cylinders in default translate mode	
02	37C8H		Specific Configuration 37C8H: Need Set Feature for spin-up after power-up Identify Device is incomplete	
03	00XXH		Number of heads in default translate mode	
04	0	*	Reserved	
05	0	*	Reserved	
06	003FH		Number of sectors per track in default translate mode	
07	0000H	*	Number of bytes in sector gap	
08	0000H	*	Number of bytes in sync field	
09	0000H	*	Reserved	
10-19	XXXX		Serial number in ASCII (0 = not specified)	
20	0003H	*	Controller type: 0003: dual ported, multiple sector buffer with look-ahead read	
21	XXXXH	*	Buffer size in 512-byte increments	
22	0034H	*	Number of ECC bytes (Vendor unique length is selected via Set Feature Command)	
23-26	XXXX		Micro code version in ASCII	
27-46	XXXX		Model number in ASCII	
47	8010H		15-8: (=80h) 7-0: Maximum number of sectors that can be transferred per interrupt on Read and Write Multiple commands.	

Table 63: Identify device information (Part 2 of 7)

An asterisk (*) in next to the Content field indicates the use of those parameters that are vendor specific

Word	Content		Description
48	0000H		Reserved
49	XF00H	*	Capabilities, bit assignments: 15-14(=0) Reserved 13 Standby timer (=1) Values as specified in ATA standard are supported (=0) Values are vendor specific 12(=0) Reserved 11(=1) IORDY Supported 10(=1) IORDY can be disabled 9(=1) Reserved 8(=0) Reserved 7-0(=0) Reserved
50	4000H		Capabilities. bit assignments 15-14(=01) Word 50 is valid 13- 1(=0) Reserved 0 Minimum value of Standby timer (=0) less than 5 minutes (=1) equal to or greater than 5 minutes
51	0200H		PIO data transfer cycle timing mode
52	0200H	*	DMA data transfer cycle timing mode. Refer to Word 62 and 63
53	0007H		Validity flag of the word 15- 3(=0) Reserved 2(=1) 1 Word 88 is Valid 1(=1) 1=Word 64-70 are Valid 0(=1) 1=Word 54-58 are Valid
54	XXXXH		Number of current cylinders
55	XXXXH		Number of current heads
56	XXXXH		Number of current sectors per track
57-58	XXXXH		Current capacity in sectors Word 57 specifies the low word of the capacity
59	0XXXH		Current Multiple setting. Bit assignments: 15- 9(=0) Reserved 8 1= Multiple Sector Setting is Valid 7- 0 xxh = Current setting for number of sectors
60-61	XXXXH		Total Number of User Addressable Sectors Word 60 specifies the low word of the number FFFFFFFh=The 48-bit native max address is greater than 268,435,455
62	0000H		
63	XX07H		Multiword DMA Transfer Capability 15- 8 Multiword DMA transfer mode active 7- 0(=7) Multiword DMA transfer modes supported (support mode 0,1,and 2

Table 64: Identify device information (Part 3 of 7)

Word	Content	Description
64	0003H	Flow Control PIO Transfer Modes Supported 15- 8(=0) Reserved 7- 0(=3) Advanced PIO Transfer Modes Supported '11' = PIO Mode 3 and 4 Supported
65	0078H	Minimum Multiword DMA Transfer Cycle Time Per Word 15- 0(=78h) Cycle time in nanoseconds (120 ns, 16.6 MB/s)
66	0078H	Manufacturer's Recommended Multiword DMA Transfer Cycle Time 15- 0(=78h) Cycle time in nanoseconds (120 ns, 16.6 MB/s)
67	00F0H	Minimum PIO Transfer Cycle Time Without Flow Control 15- 0(=F0h) Cycle time in nanoseconds (240 ns, 8.3 MB/s)
68	0078H	Minimum PIO Transfer Cycle Time With IORDY Flow Control 15- 0(=78h) Cycle time in nanoseconds (120 ns, 16.6 MB/s)
69-74	0000H	Reserved
75	00XXH	Queue depth 15- 5 Reserved 4- 0 Maximum queue depth
76-79	0000H	Reserved
80	007CH	Major version number 15- 0 (=7C) ATA-2,ATA-3,ATA/ATAPI-4,ATA/ATAPI-5,ATA/ATAPI-6
81	0019H	Minor version number 15- 0 (=19) ATA/ATAPI-6 T13 14100 Revision 3a
82	74EBH	Command set supported 15(=0) Reserved 14(=1) NOP command 13(=1) READ BUFFER command 12(=1) WRITE BUFFER command 11(=0) Reserved 10(=1) Host Protected Feature set 9(=0) DEVICE RESET command 8(=0) SERVICE interrupt 7(=1) RELEASE interrupt 6(=1) LOOK AHEAD 5(=1) WRITE CACHE 4(=0) PACKET Command Feature set 3(=1) Power Management Feature Set 2(=0) Removable feature set 1(=1) Security feature set 0(=1) SMART feature set

Table 65: Identify device information (Part 4 of 7)

Word	Content	Description
83	7BEAH	Command set supported 15-14 Word 83 is valid 13(=1) FLUSH CACHE EXT command supported 12(=1) FLUSH CACHE command supported 11(=1) Device Configuration Overlay command supported 10(=1) 48-bit Address Feature Set supported 9(=1) Automatic Acoustic mode 8(=1) SET Max Security extension 7(=1) Set Features Address Offset Feature mode 6(=1) SET FEATURES subcommand required to spin-up 5(=1) Power-Up In Standby feature set supported 4(=0) Removable Media Status Notification feature 3(=1) Advanced Power Management Feature Set 2(=0) CFA feature set 1(=1) READ/WRITE DMA QUEUED 0(=0) DOWNLOAD MICROCODE command
84	4023H	Command set/feature supported extension 15-14 Word 84 is valid 13- 6 Reserved 5 (=1) General purpose logging feature set supported 4-2 Reserved 1 (=1) SMART self-test supported 0 (=1) SMART error logging supported
85	XXXXH	Command set/feature enabled 15 Reserved 14 NOP command 13 READ BUFFER command 12 WRITE BUFFER command 11 Reserved 10 Host Protected Area Feature Set 9 DEVICE RESET command 8 SERVICE interrupt 7 RELEASE interrupt 6 LOOK AHEAD 5 WRITE CACHE 4 PACKET Command Feature Set 3 Power Management Feature Set 2 Removable Feature Set 1 Security Feature Set 0 SMART Feature Set

Table 66: Identify device information (Part 5 of 7

Word	Content	Description
86	XXXXH	Command set supported 15-14 Reserved 13 FLUSH CACHE EXT command supported 12 FLUSH CACHE command supported 11 Device Configuration Overlay command supported 10 48-bit Address Feature Set supported 9 Automatic Acoustic Management enabled 8 SET Max Security extension enabled 7 Set Features Address Offset Feature mode 6 Set Features subcommand required to spin-up after power- up 5 Power-Up In Standby feature set enabled 4 Removable Media Status Notification feature 3 Advanced Power Management Feature Set 2 CFA feature set 1 READ/WRITE DMA QUEUED 0 DOWNLOAD MICROCODE command
87	4023H	Command set/feature enabled 15-14(=01) Word 87 is valid 13- 6(=0) Reserved 5(=1) General Purpose Logging feature set supported 4-2(=0) Reserved 1(=1) SMART self-test supported 0(=1) SMART error logging supported
88	0X3FH	Ultra DMA transfer modes 15- 8(=xx Current active Ultra DMA transfer mode 15-14 Reserved (=0) 13 Mode 5 1=Active 0=Not Active 12 Mode 4 1=Active 0=Not Active 11 Mode 3 1=Active 0=Not Active 10 Mode 2 1=Active 0=Not Active 9 Mode 1 1=Active 0=Not Active 8 Mode 0 1=Active 0=Not Active 7- 0(=3F) Ultra DMA transfer mode supported 5 Mode 5 1=Support 4 Mode 4 1=Support 3 Mode 3 1=Support 2 Mode 2 1=Support 1 Mode 1 1=Support 0 Mode 0 1=Support
89	XXXXH	Time required for Security Erase Unit completion Time= value x 2 [minutes]
90	0000H	Time required for Enhanced Security Erase completion
91	0000H	Current Advanced Power Management value
92	FFFEH	Master Password Revision Code

Table 67: Identify device information (Part 6 of 7)

Word	Content	Description
93	XXXXH	Hardware reset result. Bit assignments 15-14 (=01) Word 93 is valid 13 CBLID- status 1=above Vih 0=below Vil 12- 8 Device 1 hardware reset result Device 0 clear these bits to 0 12 Reserved 11 PDIAG- assertion 1 = asset 0 = not assert 10-9 How to determine the device number: 00= Reserved 01= a jumper was used 10= the CSEL signal was used 11= some other method used or method unknown 8 Shall be set to one if Device 1 7- 0 Device 0 hardware reset result 7 Reserved 6 Respond for Device 1 1= respond 0= not respond 5 DASP- detection 1= detect 0= not detect 4 PDIAG- detection 1= pass 0= fail 3 Device 0 diagnostic 1= pass 0= fail 2-1 How to determine the device number 00=Reserved 01=Jumper 10=CSEL signal 11=Other method 0 Shall be set to one if Device 0
94	XXXXH	Current Advanced Acoustic Management value 15- 8 Vendor's Recommended Acoustic Management level 7- 0 Current Acoustic Management level
95-99	0000H	Reserved
100-103	xxxxH	Minimum user LBA address for 48-bit Address feature set
104-126	0000H	Reserved
127	0000H	Removable Media Status Notification feature set 0000H = Not supported
128	XXXXH	Security Mode Feature. Bit assignments 15-9 Reserved 8 Security Level: 1= Maximum, 0= High 7-6 Reserved 5 Enhanced erase 1= Support 4 Expire 1= Expired 3 Freeze 1= Frozen 2 Lock 1= Locked 1 Enable/Disable 1= Enable 0 Capability 1= Support

Table 68: Identify device information (Part 7 of 7)

An asterisk (*) in next to the Content field indicates the use of those parameters that are vendor specific

Word	Content		Description
129	XXXXH	*	Current Set Feature Option. Bit assignments 15-4 Reserve 3 Auto reassign 1= enabled 2 Reverting 1= enabled 1 Read Look-ahead 1= enabled 0 Write Cache 1= enabled
130-159	XXXXH	*	Reserved
160-254	0000H	*	Reserved
255	XXA5H		15- 8 Checksum. This value is the two’s complement of the sum of all bytes in byte 0 through 510 7- 0 Signature

12.9 Idle (E3h/97h)

Table 69: Idle command (E3h/97h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 0 0 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Idle command causes the device to enter Idle mode immediately and to set the auto power down time-out parameter (standby timer). And the timer then starts counting down.

When the Idle mode is entered, the device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and is ready to respond to host commands immediately.

Output parameters to the device

Sector Count Time-out Parameter. If it is zero, the automatic power down sequence is disabled. If it is nonzero, the automatic power down sequence is enabled. The time-out interval is shown below:

Value	Time-out
0	Timer disabled
1-240	Value x 5
241-251	(Value-240) x 30 minutes
252	21 minutes
253	8 hours
254	21 minutes 10 seconds
255	21 minutes 15 seconds

When the automatic power down sequence is enabled, the drive will enter Standby mode automatically if the time-out interval expires with no drive access from the host. The time-out interval will be reinitialized if there is a drive access before the time-out interval expires

12.10 Idle Immediate (E1h/95h)

Table 70: Idle Immediate command (E1h/95h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 0 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Idle Immediate command causes the device to enter Performance Idle mode.

The device is spun up to operating speed. If the device is already spinning, the spin up sequence is not executed.

During Idle mode the device is spinning and ready to respond to the host commands immediately.

The Idle Immediate command will not affect the auto power down time-out parameter.

12.11 Initialize Device Parameters (91h)

Table 71: Initialize Device Parameters command (91h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	- - - - - - - -
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D H H H H		Device/Head	- - - - - - - -
Command	1 0 0 1 0 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	0	0	-	-	0	-	V

The Initialize Device Parameters command enables the host to set the number of sectors per track and the number of heads minus 1, per cylinder. Words 54–58 in Identify Device Information reflect these parameters.

The parameters remain in effect until the following events occur:

- Another Initialize Device Parameters command is received
- The device is powered off
- A soft reset/hard reset has occurred
- The Set Feature option of CCh instead of 66h is set.

Output parameters to the device

Sector Count This indicates the number of sectors per track. Zero (0) means that there are no sectors rather than 256 sectors per track.

H This indicates the number of heads minus 1 per cylinder. The minimum is 0 and the maximum is 15.

The following condition needs to be met to avoid invalid number of cylinders beyond FFFFh:

`(Total number of user addressable sectors)/((sector count) x (H+1)) = < FFFFh`

The total number of user addressable sectors is described in Identify Device command.

12.12 NOP (00h)

Table 72: NOP Command (00h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	- - - - - - - -		Sector Count	Initial value
Sector Number	- - - - - - - -		Sector Number	Initial value
Cylinder Low	- - - - - - - -		Cylinder Low	Initial value
Cylinder High	- - - - - - - -		Cylinder High	Initial value
Device/Head	1 - 1 D - - - -		Device/Head	Initial value
Command	0 0 0 0 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	0	0	-	-	0	-	V

This command always fails with an error. The device responds with command aborted.

Output parameters to the device

Feature	**Subcommand code**
001H	Abort any outstanding queue
01H-FFH	Do not abort any outstanding queue

The value of Sector Count, Sector Number, Cylinder High/Low, Device/Head set by host is not changed.

12.13 Read Buffer (E4h)

Table 73: Read Buffer (E4h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 0 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Read Buffer command transfers a sector of data from the sector buffer of the device to the host.

The sector is transferred through the Data Register 16 bits at a time.

The sector transferred will be from the same part of the buffer written to by the last Write Buffer command. The contents of the sector may be different if any reads or writes have occurred since the Write Buffer command was issued.

12.14 Read DMA (C8h/C9h)

Table 74: Read DMA command (C8h/C9h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	1 1 0 0 1 0 0 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Read DMA command reads one or more sectors of data from disk media and then transfers the data from the device to the host. It transfers the sectors through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by the DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that the data transfer has terminated and that status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, 256 sectors will be transferred.

Sector Number This indicates the sector number of the first sector to be transferred. (L = 0).

In LBA mode, this register specifies the transfer of LBA address bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the first sector to be transferred. (L = 0).

In LBA mode, this register specifies the transfer of LBA address bits 8–15 (Low) and 16–23 (High). (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0).

In LBA mode this register specifies that LBA bits 24–27 is to be transferred. (L = 1)

R This indicates the retry bit. This bit is ignored.

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number	This indicates the sector number of the last transferred sector. (L = 0). In LBA mode this register contains the current LBA bits 0–7. (L = 1)
Cylinder High/Low	This indicates the cylinder number of the last transferred sector. (L = 0). In LBA mode this register contains the current LBA bits 8–15 (Low) and bits16–23 (High). (L=1)
H	This indicates the head number of the sector to be transferred. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

12.15 Read DMA Ext (25h)

Table 75: Read DMA Ext Command (25h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		1 1 1 0 - - - -		Device/Head		- - - - - - - -
Command		0 0 1 0 0 1 0 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	Vs	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read DMA command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. The data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output parameters to the device

Sector Count Current The number of sectors to be transferred low order, bits (7:0).

Sector Count Previous The number of sectors to be transferred high order, bits (15:8). If 0000h in the Sector Count register is specified, then 65,536 sectors will be transferred.

Sector Number Current LBA (7:0)

Sector Number Previous LBA (31:24)

Cylinder Low Current LBA (15:8)

Cylinder Low Previous LBA (39:32)

Cylinder High Current	LBA (23:16)
Cylinder High Previous	LBA (47:40)

Input parameters from the device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24)of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8)of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32)of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16)of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40)of the address of the first unrecoverable error.

12.16 Read DMA Queued (C7h)

Table 76: Read DMA command (C8h/C9h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	1 1 0 0 0 1 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

This command executes in a similar manner to a READ DMA command. The device may perform a bus release or it may execute the data transfer without performing a bus release if the data is ready to transfer.

If the device performs a bus release, the host shall reselect the device using the SERVICE command.

When the data transfer is begun, the device does not perform a bus release until the entire data transfer has been completed.

Output parameters to the device

Feature The number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.

Sector Count Bits 7 - 3 (Tag) contain the Tag for the command being delivered.

Sector Number Starting sector number or LBA address bits 7 - 0.

Cylinder High/Low Starting cylinder number or LBA address bits 23 - 8.

H Starting head number or LBA address bits 27 - 24

Input parameters from the device on bus release

Sector Count Bits 7 - 3 (Tag) contain the Tag of the command being bus released.
Bit 2 (REL) is set to one.
Bit 1 (I/O) is cleared to zero.
Bit 0 (C/D) is cleared to zero.

Sector Number, Cylinder High/low, H n/a.

SRV Cleared to zero when the device performs a bus release. This bit is set to one when the device is ready to transfer data.

Input parameters from the device on command complete

Sector Count	Bits 7 - 3 (Tag) contain the Tag of the completed command. Bit 2 (REL) is cleared to zero. Bit 1 (I/O) is set to one. Bit 0 (C/D) is set to one.

Sector Number, Cylinder High/Low, H

Sector address of unrecoverable error (applicable only when an unrecoverable error has occurred.)

SRV	Cleared to zero

12.17 Read DMA Queued Ext (26h)

Table 77: Read DMA Ext Command (25h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	V V V V V V V V		Error		see below
	Previous	V V V V V V V V				
Sector Count	Current	V V V V - - - -		Sector Count	HOB=0	V V V V V V V V
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		1 1 1 0 - - - -		Device/Head		- - - - - - - -
Command		0 0 1 0 0 1 0 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

This command executes in a similar manner to a READ DMA command. The device may perform a bus release or it may execute the data transfer without performing a bus release if the data is ready to transfer.

If the device performs a bus release, the host shall re-select the device using the SERVICE command.

When the data transfer is begun, the device does not perform a bus release until the entire data transfer has been completed.

Output parameters to the device

Feature Current The number of sectors to be transferred low order, bits (7:0).

Feature Previous The number of sectors to be transferred high order, bits (15:8). If 0000h in the Feature register is specified, then 65,536 sectors will be transferred.

Sector Count Current Bits (7:3) (Tag) contain the Tag for the command being delivered.

Sector Number Current LBA (7:0)

Sector Number Previous LBA (31:24)

Cylinder Low Current LBA (15:8)

Cylinder Low Previous LBA (39:32)

Cylinder High Current LBA (23:16)

Cylinder High Previous LBA (47:40)

Input parameters from the device on bus release

Sector Count (HOB=0)	Bits 7 - 3 (Tag) contain the Tag of the completed command. Bit 2 (REL) is cleared to zero. Bit 1 (I/O) is set to one. Bit 0 (C/D) is set to one.
Sector Number, Cylinder High/Low	n/a
SRV	Cleared to zero when the device performs a bus release. This bit is set to one when the device is ready to transfer data.

Input parameters from the device on command complete

Sector Count (HOB=0)	Bits 7 - 3 (Tag) contain the Tag of the completed command. Bit 2 (REL) is cleared to zero. Bit 1 (I/O) is set to one. Bit 0 (C/D) is set to one.
Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
SRV	Cleared to zero

12.18 Read Log Ext (2Fh)

Table 78: Read Log Ext Command (2Fh)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Cylinder High	Current	- - - - - - - -		Cylinder High	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Device/Head		1 - 1 0 - - - -		Device/Head		- - - - - - - -
Command		0 0 1 0 1 1 1 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

This command returns the specified log to the host. The device shall interrupt for each DRQ block transferred.

Output parameters to the device

Sector Count Current The number of sectors to be read from the specified log low order, bits (7:0). The log transferred by the drive shall start at the sector in the specified log at the specified offset, regardless of the sector count requested.

Sector Number Previous The number of sectors to be read from the specified log high orders, bits (15:8).

Sector Number Current The log to be returned as described in the figure below.

Cylinder Low Current The first sector of the log to be read low order, bits (7:0).

Cylinder Low Previous The first sector of the log to be read high order, bits (15:8).

Table 79: Log Address Definition

Log Address	Content	Feature set	Type
00h	Log directory	N/A	Read Only
03h	Extended Comprehensive SMART error log	SMART error logging	Ready Only
06h	SMART self-test log	SMART self-test	*See Note*
07h	Extended SMART self-test log	SMART self-test	Read Only
80h-9Fh	Host vendor specific	SMART	Read/Write

Note: If log address 06h is accessed using the Read Log Ext or Write Log Ext commands, command abort shall be returned.

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log sector shall also be included in the Comprehensive SMART self-test log sector with the 48-bit entries.

If the feature set associated with the log specified in the Sector Number register is not supported or enabled, or if the values in the Sector Count, Sector Number or Cylinder Low registers are invalid, the device shall return command aborted.

12.18.1 General Purpose Log Directory

The figure below defines the 512 bytes that make up the General Purpose Log Directory.

Table 80: General Purpose Log Directory

Description	Bytes	Offset
General purpose logging version	2	00h
Number of sectors in the log at log address 01h (7:0)	1	02h
Number of sectors in the log at log address 01h (15:8)	1	03h
Number of sectors in the log at log address 01h (7:0)	1	04h
Number of sectors in the log at log address 01h (15:8)	1	05h
...		
10h sectors in the log at log address 80h (7:0)	1	100h
00h of sectors in the log at log address 80h (7:0)	1	101h
...		
Number of sectors in the log at log address FFh (7:0)	1	1FEh
Number of sectors in the log at log address FFh (15:8)	1	1FEh
	512	

The value of the General Purpose Logging Version word shall be 0001h. A value of 0000h indicates that there is no General Purpose Log Directory.

The logs at log addresses 80-9Fh shall each be defined as 16 sectors long.

12.18.2 Extended Comprehensive SMART Error Log

The figure below defines the format of each of the sectors that comprise the Extended Comprehensive SMART error log. Error log data structure shall not include errors attributed to the receipt of faulty commands such as command codes not implemented by the device or requests with invalid parameters or in valid addresses.

Table 81: Extended Comprehensive SMART Error Log

Description	Bytes	Offset
Smart error log version	1	00h
Reserved	1	01h
Error log index (7:0)	1	02h
Error log index (15:8)	1	03h
1st error log data structure	124	04h
2nd error log data structure	124	80h
3rd error log data structure	124	FCh
4th error log data structure	124	178h
Device error count	2	1F4h
Reserved	9	1F6h
Data structure checksum	1	1FFh
	512	

12.18.2.1 Error log version

The value of this version shall be 01h.

12.18.2.2 Error log index

This indicates the error log data structure representing the most recent error. If there have been no error log entries, it is cleared to 0. Valid values for the error log index are 0 to 4.

12.18.2.3 Extended Error log data structure

An error log data structure shall be presented for each of the last four errors reported by the device. These error log data structure entries are viewed as a circular buffer. The fifth error shall create an error log structure that replaces the first error log data structure. The next error after that shall create an error log data structure that replaces the second error log structure, etc.

Unused error log data structures shall be filled with zeros.

12.18.2.3.1 Data format of extended error log data structure

Table 82: Extended Error log data structure

Description	Bytes	Offset
1st error log data structure	18	00h
2nd error log data structure	18	12h
3rd error log data structure	18	24h
4th error log data structure	18	36h
5th error log data structure	18	48h
Error data structure	34	5Ah
	124	

12.18.2.3.2 Data format of command data structure

Table 83: Command data structure

Description	Bytes	Offset
Device Control register	1	00h
Features register (7:0) (see Note)	1	01h
Features register (15:8)	1	02h
Sector count register(7:0)	1	03h
Sector count register(15:8)	1	04h
Sector number register(7:0)	1	05h
Sector number register(15:8)	1	06h
Cylinder Low register (7:0)	1	07h
Cylinder Low register (15:8)	1	08h
Cylinder High register (7:0)	1	09h
Cylinder High register (15:8)	1	0Ah
Device/Head register	1	0Bh
Command register	1	0Ch
Reserved	1	0Dh
Timestamp (milliseconds from Power-on)	4	0Eh
	18	

Note: bits (7:0) refer to the most recently written contents of the register. Bits (15:8) refer to the contents of the register prior to the most recent write to the register

12.18.2.3.3 Data format of error data structure

Table 84: Error data structure

Description	Bytes	Offset
Reserved	1	00h
Error register (7:0)	1	01h
Sector count register(7:0)(See Note)	1	02h
Sector count register(15:8)(See Note)	1	03h
Sector number register(7:0)	1	04h
Sector number register(15:8)	1	05h
Cylinder Low register (7:0)	1	06h
Cylinder Low register (15:8)	1	07h
Cylinder High register (7:0)	1	08h
Cylinder High register (15:8)	1	09h
Device/Head register	1	0Ah
Status register	1	0Bh
Extended error data (vendor specific)	19	0Ch
State	1	1Fh
Life stamp (hours)	2	20h
	34	

N*ote:* bits (7:0) refer to the contents if the register is read with bit 7 of the Device Control register cleared to zero. Bits (15:8) refer to the contents if the register is read with bit 7 of the Device Control register set to one.

State shall contain a value indicating the state of the device when the command was issued to the device or the reset occurred as described below.

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle
x4h	SMART Off-line or Self-test
x5h-xAh	Reserved
xBh-xFh	Vendor specific

12.18.2.4 Device error count

This field shall contain the total number of errors attributable to the device that have been reported by the device during the life of the device. This count shall not include errors attributed to the receipt of faulty commands such as commands codes not implemented by the device or requests with invalid parameters or invalid addresses. If the maximum value for this field is reached the count shall remain at the maximum value when additional errors are encountered and logged.

12.18.3 Extended Self-test log sector

The figure below defines the format of each of the sectors that comprise the Extended SMART self-test log.

The Extended SMART self-test log sector shall support 48-bit and 28-bit addressing. All 28-bit entries contained in the SMART self-test log, defined in 11.42.6, "Self-test log data structure" on page0203, shall also be included in the Extended SMART self-test log with all 48-bit entries.

Description	Bytes	Offset
Self-test log data structure revision number	1	00h
Reserved	1	01h
Self-test descriptor index (7:0)	1	02h
Self-test descriptor index (15:8)	1	03h
Descriptor entry 1	26	04h
Descriptor entry 2	25	1Eh
...		
Descriptor entry 18	26	1D8h
Vendor specific	2	1F2h
Reserved	11	1F4h
Data structure checksum	1	1FFh
	512	

These descriptor entries are viewed as a circular buffer. The nineteenth self-test shall create a descriptor entry that replaces descriptor entry 1. The next self-test after that shall create a descriptor entry that replaces descriptor entry 2, etc. All unused self-test descriptors shall be filled with zeros.

12.18.3.1 Self-test log data structure revision number

The value of this revision number shall be 01h.

12.18.3.2 Self-test descriptor index

This indicates the most recent self-test descriptor. If there have been no self-tests, this is set to zero. Valid values for the Self-test descriptor index are 0 to 18.

12.18.3.3 Extended Self-test log descriptor entry

The content of the self-test descriptor entry is shown below.

Description	Bytes	Offset
Self-test number	1	00h
Self-test execution status	1	01h
Power-on life timestamp in hours	2	02h
Self-test failure check point	1	04h
Failing LBA (7:0)	1	05h
Failing LBA (15:8)	1	06h
Failing LBA (23:16)	1	07h
Failing LBA (31:24)	1	08h
Failing LBA (39:32)	1	09h
Failing LBA (47:40)	1	0AH
Vendor specific	15	0BH
	26	

12.19 Read Long (22h/23h)

Table 85: Read Long (22h/23h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	0 0 0 0 0 0 0 1		Sector Count	- - - - - - - V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 0 1 0 0 0 1 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read Long command reads the designated one sector of data and the ECC bytes from the disk media. It then transfers the data and ECC bytes from the device to the host.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to transfer the ECC bytes to the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are 4 or 40 according to the setting of Set Feature option. The default setting is 4 bytes of ECC data.

The command makes a single attempt to read the data and does not check the data using ECC. Whatever is read is returned to the host.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 8–15 (Low), 16–23 (High). (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 24–27. (L = 1)

R This indicates the retry bit. This bit is ignored.

Input parameters from the device

Sector Count	This indicates the number of requested sectors not transferred
Sector Number	This indicates the sector number of the transferred sector. (L = 0)
	In LBA mode, this register contains current LBA bits 0–7. (L = 1)
Cylinder High/Low	This indicates the cylinder number of the transferred sector. (L = 0)
	In LBA mode, this register contains current LBA bits 8–15 (Low), 16–23 (High). (L = 1)
H	This indicates the head number of the transferred sector. (L = 0)
	In LBA mode, this register contains current LBA bits 24–27. (L = 1)

The device internally uses 52 bytes of ECC data on all data written or read from the disk. The 4-byte mode of operation is provided via an emulation. Use of the 52 byte ECC mode is recommended for testing the effectiveness and integrity of the ECC functions of the device.

12.20 Read Multiple (C4h)

Table 86: Read Multiple (C4h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	1 1 0 0 0 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read Multiple command reads one or more sectors of data from disk media and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. The command execution is identical to the Read Sectors command with one exception: an interrupt is generated for each block—as defined by the Set Multiple command—instead of for each sector.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 8–15 (Low), 16–23 (High). (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0)

In LBA mode, this register contains LBA bits 24–27. (L = 1)

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred. This number is zero unless an unrecoverable error occurs.

Sector Number This indicates the sector number of the transferred sector. (L = 0)

In LBA mode, this register contains current LBA bits 0–7. (L = 1)

Cylinder High/Low	This indicates the cylinder number of the transferred sector. (L = 0) In LBA mode, this register contains current LBA bits 8–15 (Low), 16–23 (High). (L = 1)
H	This indicates the head number of the transferred sector. (L = 0) In LBA mode, this register contains current LBA bits 24–27. (L = 1)

12.21 Read Multiple Ext (29h)

Table 87: Read DMA Ext Command (25h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		- 1 - D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 0 1 0 0 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read Multiple Ext command reads one or more sectors of data from disk media, then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time. Command execution is identical to the Read Sector(s) command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector.

Output parameters to the device

Sector Count Current The number of continuous sectors to be transferred low order, bits (7:0).

Sector Count Previous The number of continuous sectors to be transferred high order, bits (15:8). If 0000h in the Sector Count register is specified, 65,536 sectors will be transferred.

Sector Number Current LBA (7:0)

Sector Number Previous LBA (31:24)

Cylinder Low Current LBA (15:8)

Cylinder Low Previous LBA (39:32)

Cylinder High Current LBA (23:16)

Cylinder High Previous LBA (47:40)

Input parameters from the device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

12.22 Read Native Max ADDRESS (F8h)

Table 88: Read Native Max ADDRESS (F8h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	V V V V V V V V
Cylinder Low	- - - - - - - -		Cylinder Low	V V V V V V V V
Cylinder High	- - - - - - - -		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D - - - -		Device/Head	- - - - H H H H
Command	1 1 1 1 1 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

This command returns the native max LBA/CYL of the drive which is not effected by the Set Max ADDRESS command.

If the 48-bit native max address is greater than 268,435,455, the Read Native Max Address command returns a value of 268,435,455.

Input parameters from the device

Sector Number In LBA mode this register contains the native max LBA bits 0–7. (L = 1)

In CHS mode this register contains the native max sector number. (L = 0)

Cylinder High/Low In LBA mode this register contains the native max LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

In CHS mode this register contains the native max cylinder number. (L = 0)

H In LBA mode this register contains the native max LBA bits 24–27. (L = 1) In CHS mode this register contains the native maximum head number. (L = 0)

12.23 Read Native Max Address Ext (27h)

Table 89: Read Native Max Address Ext command (27h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	- - - - - - - -		Sector Count	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Sector Number	Current	- - - - - - - -		Sector Number	HOB=0	V V V V V V V V
	Previous	- - - - - - - -			HOB=1	V V V V V V V V
Cylinder Low	Current	- - - - - - - -		Cylinder Low	HOB=0	V V V V V V V V
	Previous	- - - - - - - -			HOB=1	V V V V V V V V
Cylinder High	Current	- - - - - - - -		Cylinder High	HOB=0	V V V V V V V V
	Previous	- - - - - - - -			HOB=1	V V V V V V V V
Device/Head		1 1 1 D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 0 0 1 1 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

This command returns the native max LBA of HDD which is not effected by Set Max Address Ext command.

Input parameters from the device

Sector Number (HOB=0) LBA (7:0) of the address of the Native max address

Sector Number (HOB=1) LBA (31:24) of the address of the Native max address

Cylinder Low (HOB=0) LBA (15:8) of the address of the Native max address

Cylinder Low (HOB=1) LBA (39:32) of the address of the Native max address

Cylinder High (HOB=0) LBA (23:16) of the address of the Native max address

Cylinder High (HOB=1) LBA (47:40) of the address of the Native max address

12.24 Read Sectors (20h/21h)

Table 90: Read Sectors Command (20h/21h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 0 1 0 0 0 0 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read Sectors command reads one or more sectors of data from disk media and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs the read will be terminated at the failing sector.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, 256 sectors will be transferred.

Sector Number This is the sector number of the first sector to be transferred. (L =0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This is the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This is the head number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This is the retry bit, but this bit is ignored.

Input parameters from the device

Sector Count This is the number of requested sectors not transferred. This will be zero, unless an unrecoverable error occurs.

Sector Number This is the sector number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low	This is the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This is the head number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

12.25 Read Sector(s) Ext (24h)

Table 91: Read Sector(s) Ext command (24h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		1 1 1 D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 0 0 1 0 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read Sector(s) Ext command reads from 1 to 65,536 sectors of data from disk media and then transfers the data from the device to the host.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the read will be terminated at the failing sector.

Output parameters to the device

Sector Count Current The number of continuous sectors to be transferred low order, bits (7:0).

Sector Count Previous The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, 65,536 sectors will be transferred.

Sector Number Current LBA (7:0)

Sector Number Previous LBA (31:24)

Cylinder Low Current LBA (15:8)

Cylinder Low Previous LBA (39:32)

Cylinder High Current LBA (23:16)

Cylinder High Previous LBA (47:40)

Input parameters from the device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

12.26 Read Verify Sectors (40h/41h)

Table 92: Read Verify Sectors (40h/41h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 0 1 0 0 0 0 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read Verify Sectors command verifies one or more sectors on the device. No data is transferred to the host.

The difference between the Read Sector(s) command and the Read Verify Sector(s) command is whether data is transferred to the host or not.

If an uncorrectable error occurs, the read verify will be terminated at the failing sector.

Output parameters to the device

Sector Count This is the number of continuous sectors to be verified. If zero is specified, 256 sectors will be verified.

Sector Number This is the sector number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This is the cylinder number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This is the head number of the first sector to be transferred. (L = 0)

In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This is the retry bit. this bit is ignored.

Input parameters from the device

Sector Count This is the number of requested sectors not verified. This number will be zero unless an unrecoverable error occurs.

Sector Number This is the sector number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low	This is the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This is the head number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

12.27 Read Verify Sector(s) (42h)

Table 93: Read Verify Sector(s) command (42h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		1 1 1 D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 0 0 0 1 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The Read Verify Sector(s) Ext command verifies one or more sectors on the device. No data is transferred to the host.

The difference between the Read Sector(s) command and the Read Verify Sector(s) command is whether data is transferred to the host or not.

If an uncorrectable error occurs, the Read Verify Sector(s) Ext will be terminated at the failing sector.

Output parameters to the device

Sector Count Current The number of continuous sectors to be verified low order, bits (7:0).

Sector Count Previous The number of continuous sectors to be verified high order, bits (15:8). If zero is specified in the Sector Count register, 65,536 sectors will be transferred.

Sector Number Current LBA (7:0)

Sector Number Previous LBA (31:24)

Cylinder Low Current LBA (15:8)

Cylinder Low Previous LBA (39:32)

Cylinder High Current LBA (23:16)

Cylinder High Previous LBA (47:40)

Input parameters from the device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

12.28 Recalibrate (1xh)

Table 94: Recalibrate (1xh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	0 0 0 1 - - - -		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	V	0		0	V	0	V	-	0	-	V

The Recalibrate command moves the read/write heads from anywhere on the disk to cylinder 0.

If the device cannot reach cylinder 0, T0N (Track 0 Not Found) will be set in the Error Register.

12.29 Security Disable Password (F6h)

Table 95: Security Disable Password (F6h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 1 0 1 1 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Security Disable Password command disables the security mode feature (device lock function).

The Security Disable Password command requests a transfer of a single sector of data from the host including information specified in the table below. The device then checks the transferred password. If the User Password or Master Password matches the given password, the device disables the security mode feature (device lock function). This command does not change the Master Password which may be reactivated later by setting User Password. This command should be executed in device unlock mode.

Table 96: Password Information for Security Disable Password command

Word	Description
00	Control word bit 0 : Identifier (1-Master, 0- User) bits 1-15 : Reserved
01-16	Password (32 bytes)
17- 255	Reserved

The device will compare the password sent from this host with that specified in the control word.

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

12.30 Security Disable Password (F3h)

Table 97: Security Disable Password (F3h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 1 0 0 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Security Erase Prepare command must be issued immediately before the Security Erase Unit command to enable device erasing and unlocking.

The Security Erase Prepare Command must be issued immediately before the Format Unit Command. This command is to prevent accidental erasure of the device.

This command does not request the transfer of data.

12.31 Security Erase Unit (F4h)

Table 98: Security Erase Unit (F4h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 1 0 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Security Erase Unit command initializes all user data sectors and then disables the device lock function.

Note that the Security Erase Unit command initializes from LBA 0 to Native MAX LBA. The Host MAX LBA is set by the Initialize Drive Parameter or the Set MAX ADDRESS command is ignored. The protected area by the Set MAX ADDRESS command is also initialized.

This command requests the transfer of a single sector of data from the host including information specified in the table below.

If the password does not match, the device rejects the command with an Aborted error.

Table 99: Erase Unit information

Word	Description
00	Control Word bit 0 : Identifier (1- Master, 0- User) bit 1 : Erase mode (1- Enhanced, 0 - Normal) [Enhanced mode is not supported] bit 2-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Identifier Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

The Security Erase Unit command erases all user data and disables the security mode feature (device lock function). After the completion of this command, all the user data will be initialized to zero with a write operation. At this time, the data write is not verified with a read operation to determine if the data sector is initialized correctly. At this time the defective sector information and the reassigned sector information for the device are not updated. The security erase prepare command should be completed immediately prior to the Security Erase Unit command.

If the device receives a Security Erase Unit command without a prior Security Erase Prepare command the device aborts the security erase unit command.

This command disables the security mode feature (device lock function), however, the master password is still stored internally within the device and may be reactivated later when a new user password is set. If you execute this command when disabling the security mode feature (device lock function), the password sent by the host is NOT compared with either the Master Password or the User Password. The device then erases all user data.

The execution time of this command is set in word 89 of Table 62, “Identify device information (Part 1 of 7),” on page 120.

12.32 Security Freeze Lock (F5h)

Table 100: Security Freeze Lock command (F5h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 1 0 1 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Security Freeze Lock Command allows the device to enter frozen mode immediately.

After this command is completed, the command which updates Security Mode Feature (Device Lock Function) is rejected.

Frozen mode is quit only by a Power off.

The following commands are rejected when the device is in frozen mode:

- Security Set Password
- Security Unlock
- Security Disable Password
- Security Erase Unit

Refer to Table 47: “Command table for device lock operation” on page 86.

12.33 Security Set Password (F1h)

Table 101: Security Set Password command (F1h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 1 0 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Security Set Password command enables the security mode feature (device lock function) and sets the master password or the user password.

The security mode feature (device lock function) is enabled by this command and the device is not locked immediately. The device is locked after the next power on reset or hard reset. When the MASTER password is set by this command, the master password is registered internally. The device is NOT locked after next power on reset or hard reset.

This command requests the transfer of a single sector of data from the host including the information specified in the table below.

The data transferred controls the function of this command.

Table 102: Security Set Password Information

Word	Description
00	Control Word bit 0 : Identifier (1-Master, 0-User) bit 1-7 : Reserved bit 8 : Security level (1-Maximum, 0-High) bit 9-15 : Reserved
01-16	Password (32 bytes)
17	Master Password Revision Code (valid if Word 0 bit 0 = 1)
18-255	Reserved

Identifier
Zero indicates that the device should check the supplied password against the user password stored internally. One indicates that the device should check the given password against the master password stored internally.

Security Level
Zero indicates High level. One indicates Maximum level. If the host sets High level and the password is forgotten, the Master Password can be used to unlock the device. If the host sets Maximum level and the user password is forgotten, only a Security Erase Prepare/Security Unit command can unlock the device and all data will be lost.

Password
All 32 bytes of the text of the password are always significant.

Master Password Revision Code
The Revision Code field is set with Master password. If Identifier is User, the Revision Code is not set. The Revision Code field is returned in Identify Device word 92. The valid Revision Codes are 0000h to FFFDh. The Default Master Password Revision Code is FFFEh. The code FFFFh is reserved.

Identifier and Security level bits
The setting of the Identifier and Security level bits interact as follows:

Identifier = User / Security level = High
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The drive may then be unlocked by either the user password or the previously set master password.

Identifier = Master / Security level = High
This combination will set a master password but will NOT enable the security mode feature (lock function).

Identifier = User / Security level = Maximum
The password supplied with the command will be saved as the new user password. The security mode feature (lock function) will be enabled from the next power on. The drive may then be unlocked by only the user password. The master password previously set is still stored in the drive but may NOT be used to unlock the device.

Identifier = Master / Security level = Maximum
This combination will set a master password but will NOT enable the security mode feature (lock function).

12.34 Security Unlock (F2h)

Table 103: Security Unlock command (F2h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 1 0 0 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

This command unlocks the password and causes the device to enter device unlock mode. If a power on reset or hard reset is done without executing the Security Disable Password command after this command is completed, the device will be in device lock mode. The password has not been changed yet.

The Security Unlock command requests the transfer of a single sector of data from the host including information specified in the table below.

If the Identifier bit is set to master and the drive is in high security mode, the password supplied will be compared with the stored master password. If the drive is in maximum security mode, the security unlock will be rejected.

If the Identifier bit is set to user, the drive compares the supplied password with the stored user password.

If the password compare fails, the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to five and is decremented for each password mismatch. When this counter reaches zero, all password protected commands are rejected until there is a hard reset or a power off.

Word	Description
00	Control Word bit 0 : Identifier (1- Master, 0- User) bit 1-15 : Reserved
01-16	Password (32 bytes)
17-255	Reserved

Identifier
A zero indicates that the device regards Password as the User Password. A one indicates that the device regards Password as the Master Password.

The user can detect if the attempt to unlock the device has failed due to a mismatched password since this is the only reason that an abort error will be returned by the drive AFTER the password information has been sent to the device. An abort error returned by the device BEFORE the password data has been sent to the drive indicates that another problem exists.

12.35 Seek (7xh)

Table 104: Seek command (7xh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 1 1 1 - - - -		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Seek command initiates a seek to the designated track and selects the designated head. The device does not need to be formatted for a seek to execute properly.

Output parameters to the device

Sector Number In LBA mode this register specifies the LBA address bits 0–7 for seek. (L = 1)

Cylinder High/Low This is the cylinder number of the seek. In LBA mode this register specifies the LBA address bits 8–15 (Low) and bits 16–23 (High) for seek. (L = 1)

H This is the head number of the seek. In LBA mode this register specifies the LBA address bits 24–27 for seek. (L = 1)

Input parameters from the device

Sector Number In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low In LBA mode this register contains the current LBA bits 8–15 (Low) and bits16–23 (High). (L = 1)

H In LBA mode this register contains the current LBA bits 24–27. (L = 1)

12.36 Service (A2h)

Table 105: Service command (A2h)

Command Block Output Registers	
Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -
Feature	- - - - - - - -
Sector Count	- - - - - - - -
Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -
Command	1 1 1 1 0 0 0 0

The Service command is used to provide data transfer or status or both of a command that was previously bus released.

Output parameters to the device

D Selected device

Input parameters from the device

Input from the device as a result of a Service command are described in the command description for the command for which Service is being requested.

12.37 Set Features (EFh)

Table 106: Set Features command (EFh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	see note 1		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 1 1 1 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Set Feature command establishes the following parameters which affect the execution of certain features as shown in the table below.

ABT will be set to 1 in the Error Register if the Feature register contains any undefined values.

Output parameters to the device

02H	Enable write cache
03H	Set transfer mode based on value in sector count register
05H	Enable Advanced Power Management
06H	Enable Power-up in Standby feature set
07H	Power-up in Standby feature set device spin-up
09H	Enable Address Offset mode
42H	Enable Automatic Acoustic Management
44H	52 bytes of ECC apply on Read Long/Write Long commands
55H	Disable read look-ahead feature
5DH	Enable release interrupt
66H	Disable reverting to power on defaults
82H	Disable write cache
85H	Disable Advanced Power Management
86H	Disable Power-up in Standby mode
89H	Disable Address Offset mode
AAH	Enable read look-ahead feature
BBH	4 bytes of ECC apply on Read Long/Write Long commands
C2H	Disable Automatic Acoustic Management
CCH	Enable reverting to power on defaults
DDH	Disable release interrupt

Note: After the power on reset or hard reset the device is set to the following features as default.

Write cache	Enable
ECC bytes	4 bytes
Read look-ahead	Enable
Reverting to power on defaults	Disable
Release interrupt	Disable

12.37.1 Set Transfer mode

When the Feature register is 03h (= Set Transfer mode) the Sector Count Register specifies the transfer mechanism. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

PIO Default Transfer Mode	00000 000
PIO Default Transfer Mode, Disable IORDY	00000 001
PIO Flow Control Transfer Mode x	00001 nnn (nnn=000,001,010,011,100)
Multiword DMA mode x	00100 nnn (nnn=000,001,010)
Ultra DMA mode x	01000 nnn (nnn=000,001,010,011,100,101)

12.37.2 Write Cache

If the number of auto reassigned sectors reaches the reassignment capacity of the device, the write cache function will automatically be disabled. Although the device still accepts the Set Features command (with Feature register = 02h) without error, the write cache function will remain disabled. For the current write cache function status, refer to (word 85 or 129) in Table 62: "Identify device information (Part 1 of 7)" on page 120.

12.37.3 Advanced Power Management

When the Feature Register is 05h (=Enable Advanced Power Management) the Sector Count Register specifies the Advanced Power Management level.

FFH	Aborted
C0-FEh	The lowest Power Saving Mode is Normal Idle mode (the same as Disable Advanced Power Management)
80-BFh	The lowest power consumption mode is Low Power Idle
01-7Fh	The lowest power consumption mode is Low RPM standby mode
00H	Aborted

The idle time to Low power idle mode and Low RPM standby mode vary according to the value in Sector Count register as follows:

When Low power idle mode is the deepest Power Saving mode,

$y_1 = (x - 80h) * 5 + 120$[sec] $(120 \leq y_1 \leq 435)$

$y_2 =$ N/A (the device does not go to Low RPM standby mode)

When Low RPM standby mode is the deepest Power Saving mode and the value in Sector Count register is between 40h and 7Fh,

$120 \leq y_1 \leq 435$ [sec] (default: 120 [sec])

$y_2 = (x - 40h) * 60 + 600$ [sec] $(600 \leq y_2 \leq 4380)$

When Low RPM standby mode is the deepest Power Saving Mode and the value in Sector Count register is between 01h and 3Fh,

where

$120 \leq y_1 \leq 435$ [sec] (default: 120 [sec])

$y_2 = 600$ [sec]

x = the value in Sector Count register

y1 = the idle time to Low Power Idle mode

y2 = the idle time to Low RPM standby mode

If Low power idle mode has already been enabled (i.e., y1 has been set) before Low RPM standby mode is enabled, y1 is preserved. If Low power idle mode is disabled (i.e., y1 has not yet been set), y1 becomes 120 seconds when Low RPM standby mode is enabled.

Enabled Power Saving mode and idle time (y1 and y2) are preserved until Advanced Power Management is disabled, the deepest Power Saving mode becomes Normal Idle mode, or a new time is set. They are initialized with a hard/soft reset unless Reverting to Power on defaults is disabled and the devise receives a soft reset.

Additional electronics are powered off and the heads are unloaded on the ramp. The spindle is still rotated at the full speed.

The heads are unloaded on the ramp and the spindle is rotated at the 60-65% of the full speed.

When Feature register is 85h (= Disable Advanced Power Management), the deepest Power Saving becomes normal Idle.

12.37.4 Automatic Acoustic Management

When Feature register is 42h (= Enable Automatic Acoustic Management), the Sector Count Register specifies the Automatic Acoustic Management level.

FFH	Aborted
C0-FEh	Set to Normal Seek mode
80-BFh	Set to Quiet Seek mode
00- 7Fh	Aborted

The device preserves enabling or disabling of Automatic Acoustic Management and the current Automatic Acoustic Management level setting across all forms of reset, that is, Power on, Hardware, and Software Resets.

12.38 Set Max ADDRESS (F9h)

Table 107: Set Max ADDRESS command (F9h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	- - - - - - - B		Sector Count	- - - - - - - -
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	1 1 1 1 1 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

If this command is immediately preceded by a Read Native Max Address command, the device regards it as a Set Max Address command. The device receives this command without a prior Read Native Max Address command and regards it as a Set Max security extensions command according to feature register value.

Valid features values are as shown below:

- 01h indicates Set Max Set Password command
- 02h indicates Set Max Lock command
- 03h indicates Set Max Unlock command
- 04h indicates Set Max Freeze LOCK command

This command overwrites the maximum number of Addresses of the drive in a range of actual device capacity. When the device receives this command, all accesses beyond that Address are rejected with setting ABORT bit in status register. Identify Device Command returns the Address which is set via this command as a default value.

If the device in Address Offset mode receives this command with the nonvolatile option, the device returns aborted error to the host.

The device returns command aborted for a second nonvolatile Set Max Address command until the next power on or hardware reset.

The device returns command aborted during Set Max Locked mode or Set Max Frozen mode.

After a successful command completion, Identify Device response words (61:60) shall reflect the maximum address set with this command.

If the 48-bit Address feature set is supported, the value placed in Identify Device response words (103:100) shall be the same as the value placed in words (61:60). However, if the device contains greater than 268,435,455 sectors, the capacity addressable with 28-bit commands, and the address requested is 268,435,455, the max address shall be changed to the native maximum address, the value placed in words (61:60) shall be 268,435,455 and the value placed in words (103:100) shall be the native maximum address.

If a host protected area has been established by a Set Max Address Ext command, the device shall return command aborted.

Output parameters to the device

B	Option bit for selection whether nonvolatile or volatile. B = 0 is volatile condition. When B=1, MAX LBA/CYL which is set by Set Max LBA/CYL command is preserved by POR. When B=0, MAX LBA/CYL which is set by Set Max LBA/CYL command will be lost by POR. B = 1 is not valid when the device is in Address Offset mode.
Sector Number	In LBA mode this register contains LBA bits 0 - 7 which is to be set. (L=1) In CHS mode this register is ignored. (L=0)
Cylinder High/Low	In LBA mode this register contains LBA bits 8 - 15 (Low), 16 - 23 (High) which is to be set. (L=1) In CHS mode this register contains cylinder number which is to be set. (L=0)
H	In LBA mode this register contains LBA bits 24 - 27 which is to be set. (L=1) In CHS mode this register is ignored. (L=0)

Input parameters from the device

Sector Number	In LBA mode this register contains max LBA bits 0 - 7 which is set. (L=1) In CHS mode this register contains max sector number. (L=0)
Cylinder High/Low	In LBA mode this register contains max LBA bits 8 - 15 (Low), 16 - 23 (High) which is set. (L=1) In CHS mode this register contains max cylinder number which is set. (L=0)
H	In LBA mode this register contains max LBA bits 24 - 27 which is set. (L=1) In CHS mode this register contains max head number. (L=0)

12.38.1 Set Max Set Password (Feature=01h)

Table 108: Set Max Set Password command

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	0 0 0 0 0 0 0 1		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	1 - 1 D - - - -
Command	1 1 1 1 1 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

If this command is immediately preceded by a Read Native Max Address command, the device regards it as a Set Max Address command

This command requests a transfer of a single sector of data from the host including the information specified in the figure below.

The password is retained by the device until the next power cycle. When the device accepts this command, the device is in Set_Max_Unlocked state.

Table 109: Set Max Set Password data contents

Word	Description
00	Reserved
01-16	Password (32 bytes)
17-255	Reserved

12.38.2 Set Max Lock (Feature=02h)

Table 110: Set Max Lock command

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	0 0 0 0 0 0 1 0		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	1 - 1 D - - - -
Command	1 1 1 1 1 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

If this command is immediately preceded by a Read Native Max Address command, the device regards it as a Read Native Max Address command.

This command sets the device into Set_Max_Locked state. After this command is completed, any other Set Max commands except Set Max Unlock and Set Max Freeze Lock are rejected. The device remains in this state until a power cycle or the acceptance of a Set Max Unlock or Set Max Freeze Lock command

12.38.3 Set Max Unlock (Feature = 03h)

Table 111: Set Max Unlock command (F9h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	0 0 0 0 0 0 1 0		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	1 - 1 D - - - -
Command	1 1 1 1 1 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

If this command is immediately preceded by a Read Native Max Address command, the device regards it as Set Max Address command

This command requests a transfer of a single sector of data from the host including the information specified in Table 108: “Set Max Set Password command” on page 178 with the stored SET MAX password.

If the password compare fails, the device returns an abort error to the host and decrements the unlock attempt counter. This counter is initially set to 5 and is decremented for each password mismatch. When this counter reaches zero, all Set Max Unlock commands are rejected until a hard reset or a power off occurs.

If the password compare matches, the device sets the Set_Max_Unlocked state and all Set Max commands are accepted.

12.38.4 Set Max Freeze Lock (Feature = 04h)

Table 112: Set Max Freeze Lock (F9h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	0 0 0 0 0 0 1 0		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	1 - 1 D - - - -
Command	1 1 1 1 1 0 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

If the Set Max Freeze Lock command is immediately preceded by a Read Native Max Address command, this command is regarded as a Set Max Address command.

The Set Max Freeze Lock command sets the device to Set_Max_Frozen state. After the completion of the command any subsequent Set Max commands are rejected. The following commands are disabled by Set Max Freeze Lock:

- Set Max Address
- Set Max Set PASSWORD
- Set Max Lock
- Set Max Unlock

12.39 Set Max Address Ext (37h)

Table 113: Set Max Address Ext command (37h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	- - - - - - - B		Sector Count	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		- 1 - D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 1 0 1 1 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

This command is immediately preceded by a Read Native Max Address Ext command.

This command overwrites the maximum number of Address of HDD in a range of actual device capacity. Once the device receives this command, all accesses beyond that Address are rejected with setting ABORT bit in status register.

When the address requested is greater than 268,435,455, words (103:100) shall be modified to reflect the requested value, but words (61:60) shall not be modified. When the address requested is equal to or less than 268,435,455, words (103:100) shall be modified to reflect the requested value, and words (61:60) shall also be modified.

If this command is not supported, the maximum value to be set exceeds the capacity of the device, a host protected area has been established by a Set Max Address command, the command is not immediately preceded by a Read Native Max Address Ext command, or the device is in the Set Max Locked or Set Max Frozen state, the device shall return command aborted.

If the device in Address Offset mode receives this command with the nonvolatile option, the device returns aborted error to the host.

The device returns the command aborted for a second non-volatile Set Max Address Ext command until next power on or hardware reset.

Output parameters to the device

B	Option bit for selection whether nonvolatile or volatile. B=0 is volatile condition. When B=1, MAX Address which is set by the Set Max Address Ext command is preserved by POR. When B=0, MAX Address which is set by the Set Max Address Ext command will be lost by POR. B=1 is not valid when the device is in Address Offset mode.
Sector Number Current	Set Max LBA (7:0)
Sector Number Previous	Set Max LBA (31:24)
Cylinder Low Current	Set Max LBA (15:8)
Cylinder Low Previous	Set Max LBA (39:32)
Cylinder High Current	Set Max LBA (23:16)
Cylinder High Previous	Set Max LBA (47:40)

Input parameters from the device

Sector Number (HOB=0)	Set Max LBA (7:0).
Sector Number (HOB=1)	Set Max LBA (31:24).
Cylinder Low (HOB=0)	Set Max LBA (15:8).
Cylinder Low (HOB=1)	Set Max LBA (39:32).
Cylinder High (HOB=0)	Set Max LBA (23:16).
Cylinder High (HOB=1)	Set Max LBA (47:40).

12.40 Set Multiple (C9h)

Table 114: Set Multiple command (C6h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 0 0 0 1 1 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Set Multiple command enables the device to perform Read and Write Multiple commands and establishes the block size for these commands. The block size is the number of sectors to be transferred for each interrupt.

If an invalid block size is specified, an Abort error will be returned to the host. The Read Multiple and Write Multiple commands will be disabled.

Output parameters to the device

Sector Count This indicates the block size to be used for the Read Multiple and the Write Multiple commands. Valid block sizes can be selected from 0, 1, 2, 4, 8, or 16. If 0 is specified, then the Read Multiple and the Write Multiple commands are disabled.

12.41 Sleep (E6h/99h)

Table 115: Sleep command (E6h/99h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 0 1 1 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

This command causes the device to enter Sleep Mode.

The device is spun down and the interface becomes inactive. If the device is already spun down, the spin down sequence is not executed.

A software reset or a hardware reset is the only way to recover from Sleep Mode.

12.42 S.M.A.R.T. Function Set (B0h)

Table 116: S.M.A.R.T. Function Set command (B0h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	0 1 0 0 1 1 1 1		Cylinder Low	- - - - - - - -
Cylinder High	1 1 0 0 0 0 1 0		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 0 1 1 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

The S.M.A.R.T. Function Set command provides access to the Attribute Values, the Attribute Thresholds, and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The S.M.A.R.T. Function Set command has several separate subcommands which can be selected via the Features Register of the device when the S.M.A.R.T. Function Set command is issued by the host.

In order to select a subcommand the host must write the subcommand code to the Features Register of the device before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

12.42.1 S.M.A.R.T. Function Subcommands

Code	Subcommand
D0h	S.M.A.R.T. Read Attribute Values
D1h	S.M.A.R.T. Read Attribute Thresholds
D2h	S.M.A.R.T. Enable/disable Attribute Autosave
D3h	S.M.A.R.T. Save Attribute Values
D4h	S.M.A.R.T. Execute Off-line Immediate
D5h	S.M.A.R.T. Read Log Sector
D6h	S.M.A.R.T. Write Log Sector
D8h	S.M.A.R.T. Enable Operations
D9h	S.M.A.R.T. Disable Operations
DAh	S.M.A.R.T. Return Status
DBh	S.M.A.R.T. Enable/Disable Automatic Off-line

12.42.1.1 S.M.A.R.T. Read Attribute Values (subcommand D0h)

This subcommand returns the Attribute Values of the device to the host. Upon receipt of the S.M.A.R.T. Read Attribute Values subcommand from the host, the device saves any updated Attribute Values to the Attribute Data sectors and then transfer the 512 bytes of Attribute Value information to the host.

12.42.1.2 S.M.A.R.T. Read Attribute Thresholds (subcommand D1h)

This subcommand returns the Attribute Thresholds of the device to the host. Upon receipt of the SMART Read Attribute Thresholds subcommand from the host, the device reads the Attribute Thresholds from the Attribute Threshold sectors and then transfers the 512 bytes of Attribute Thresholds information to the host.

12.42.1.3 S.M.A.R.T. Enable/Disable Attribute Autosave (subcommand D2h)

This subcommand enables and disables the Attribute Autosave feature of the device. The S.M.A.R.T. Enable/Disable Attribute Autosave subcommand allows the device to automatically save its updated Attribute Values to the Attribute Data Sector periodically or causes the Autosave feature to be disabled. The state of the Attribute Autosave feature—either enabled or disabled—will be preserved by the device across the power cycle.

A value of 00h written by the host into the Sector Count Register of the device before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during another normal operation such as a power-up or a power-down.

A value of F1h written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand will cause this feature to be enabled. Any other nonzero value written by the host into this register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand will not change the current Autosave status. However the device will respond with the error code specified in Table 127: “S.M.A.R.T. Error Codes” on page 198.

The S.M.A.R.T. Disable Operations subcommand disables the Autosave feature along with the S.M.A.R.T. operations of the device.

Upon the receipt of the subcommand from the host, the device asserts BSY, enables or disables the Autosave feature, clears BSY, and asserts INTRQ.

12.42.1.4 S.M.A.R.T. Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the S.M.A.R.T. Save Attribute Values subcommand from the host, the device asserts BSY, writes any updated Attribute Values to the Attribute Data sector, clears BSY, and asserts INTRQ.

12.42.1.5 S.M.A.R.T. Execute Off-line Immediate (subcommand D4h)

This subcommand causes the device to immediately initiate the set of activities that collect Attribute data in an off-line mode (off-line routine) or execute a self-test routine in either captive or off-line mode. The Sector Number register shall be set to specify the operation to be executed.

Sector Number	Operation to be executed
0	Execute S.M.A.R.T. off-line data collection routine immediately
1	Execute S.M.A.R.T. Short self-test routine immediately in off-line mode
2	Execute S.M.A.R.T. Extended self-test routine immediately in off-line mode
127	Abort off-line mode self-test routine
129	Execute S.M.A.R.T. Short self-test routine immediately in captive mode
130	Execute S.M.A.R.T. Extended self-test routine immediately in captive mode

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the

host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine the device sets the execution result in the Self-test execution status byte (see Table 117: "Device Attribute Data Structure" on page 190) and ATA registers as defined below and then executes the command completion.

Status	Set ERR to one when the self-test has failed
Error	Set ABRT to one when the self-test has failed
Cyl Low	Set to F4h when the self-test has failed
Cyl High	Set to 2Ch when the self-test has failed

12.42.1.6 S.M.A.R.T. Read Log Sector (subcommand D5h)

This command returns the specified log sector contents to the host.

The 512 bytes of data are returned at a command and the Sector Count value shall be set to one. The Sector Number shall be set to specify the log sector address.

Log sector address	Content	Type
00h	Log directory	Read Only
01h	S.M.A.R.T. Error Log	Read Only
03h	Extended Comprehensive SMART Error Log	*See note*
06h	S.M.A.R.T. Self-test Log	Read Only
07h	Extended Self-test Log	*See note*
80h-9Fh	Host vendor specific	Read/Write

Note: Log addresses 03h and 07h are used by the Read Log Ext and Write Log Ext commands. If these log addresses are used with the SMART Read Log Sector command, the device shall return command aborted.

12.42.1.7 S.M.A.R.T. Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector.

The 512 bytes of data are transferred at a command and the Sector Count value shall be set to one. The Sector Number shall be set to specify the log sector address as shown above. If a Read Only log sector is specified, the device returns ABRT error.

12.42.1.8 S.M.A.R.T. Enable Operations (subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of a S.M.A.R.T. Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T.—either enabled or disabled—will be preserved by the device across power cycles. When enabled, the receipt of subsequent S.M.A.R.T. Enable Operations subcommands will not affect any of the Attribute Values.

Upon receipt of the SMART Enable Operations subcommand from the host the device enables S.M.A.R.T. capabilities and functions and then saves any updated Attribute Values to the Attribute Data sector.

12.42.1.9 S.M.A.R.T. Disable Operations (subcommand D9h)

This subcommand disables all S.M.A.R.T. capabilities within the device including the attribute Autosave feature of the device. After receipt of this subcommand the device disables all S.M.A.R.T. operations. Non self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T.—either enabled or disabled—is preserved by the device across power cycles.

Upon receipt of the S.M.A.R.T. Disable Operations subcommand from the host, the device asserts BSY, disables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

After receipt of the device of the S.M.A.R.T. Disable Operations subcommand from the host, all other S.M.A.R.T. subcommands—with the exception of S.M.A.R.T. Enable Operations—are disabled and invalid and will be aborted by the device—including the S.M.A.R.T. Disable Operations subcommand—returning the error code as specified in Table 127: "S.M.A.R.T. Error Codes" on page 198.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the S.M.A.R.T. Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a S.M.A.R.T. Read Attribute Values or a S.M.A.R.T. Save Attribute Values command.

12.42.1.10 S.M.A.R.T. Return Status (subcommand DAh)

This command is used to communicate the reliability status of the device upon the request of the host. Upon receipt of the SMART Return Status subcommand the device saves any updated Pre-failure type Attribute Values to the reserved sector and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, the device loads 4Fh into the Cylinder Low register and C2h into the Cylinder High register.

If the device detects a Threshold Exceeded Condition, the device loads F4h into the Cylinder Low register and 2Ch into the Cylinder High register.

12.42.1.11 S.M.A.R.T. Enable/Disable Automatic Off-line (subcommand DBh)

This subcommand enables and disables the optional feature that causes the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then saves this data to the non-volatile memory of the device. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the Automatic Off-line Data Collection feature to be disabled.

A value of zero written by the host into the Sector Count register of the device before issuing this subcommand causes the feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F8h written by the host into the Sector Count register of the device before issuing this subcommand causes this feature to be enabled. Any other nonzero value written by the host into this register before issuing this subcommand is vender specific and does not change the current Automatic Off-line Data Collection status, but the device may respond with the error code specified in Table 127: "S.M.A.R.T. Error Codes" on page 198.

12.42.2 Device Attribute Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Values subcommand. All multibyte fields shown in these data structures are in byte ordering, that is, the least significant byte occupies the lowest numbered byte address location in the field.

Table 117: Device Attribute Data Structure

Description	Byte	Offset	Format	Value
Data Structure Revision Number	2	00h	binary	0010h
1st Device Attribute	12	02h	(*1)	
...				
30th Device Attribute	12	15Eh	(*1)	
Off-line data collection status	1	16Ah	(*1)	
Self-test execution status	1	16Bh	(*1)	
Total time in seconds to complete off-line data collection activity	2	16Ch	(*1)	
Current segment pointer	1	16Eh	(*1)	
Off-line data collection capability	1	16Fh	(*1)	1Bh
S.M.A.R.T. capability	2	170h	(*1)	0003h
S.M.A.R.T. device error logging capability	1	172h	(*1)	01h
Self-test failure check point	1	173h	(*1)	
Short self-test completion time in minutes	1	174h	(*1)	
Extended self-test completion time in minutes	1	175h	(*1)	
Reserved	12	176h		
Vendor specific	125	182h		
Data structure checksum	1	1FFh	(*1)	
	512			

12.42.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

12.42.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

Table 118: Individual Attribute Data Structure

Description	Byte	Offset
Attribute ID Number (01h to FFh)	1	00h
Status Flags	2	01h
Attribute Value (valid values from 01h to FDh)	1	03h
Vendor Specific	8	04h
Total Bytes	12	

Attribute ID Numbers: Any nonzero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers.

ID	Attribute Name
0	Indicates that this entry in the data structure is not used
1	Raw Read Error Rate
2	Throughput Performance
3	Spin Up Time
4	Start/Stop Count
5	Reallocated Sector Count
7	Seek Error Rate
8	Seek Time Performance
9	Power-On Hours Count
10	Spin Retry Count
12	Device Power Cycle Count
192	Power Off Retract Count
193	Load Cycle Count
194	Device Temperature
196	Reallocation Event Count
197	Current Pending Sector Count
198	Off-Line Scan Uncorrectable Sector Count
199	Ultra DMA CRC Error Count

Status Flag Definition

Bit Definition

0 Pre-failure/advisory bit
- **0** An attribute value less than or equal to its corresponding attribute threshold indicates an advisory condition where the usage or age of the device has exceeded its intended design life period.
- **1** An attribute value less than or equal to its corresponding attribute threshold indicates a pre-Failure condition where imminent loss of data is being predicted

1 On-line Collective bit
- **0** The attribute value is updated only during Off-line testing.
- **1** The attribute value is updated during On-line testing or during both On-line and Off-line testing.

2 - 5 Vendor specific

6-15 Reserved (0)

Normalized values: The device performs conversion of the raw Attribute Values to transform them into normalized values which the host can then compare with the Threshold values. A Threshold is the excursion limit for a normalized Attribute Value.

12.42.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates an Automatic Off-line Data Collection Status.

Bit 7	Automatic Off-line Data Collection Status
0	Automatic Off-line Data Collection is disabled.
1	Automatic Off-line Data Collection is enabled.

Bits 0–6 represent a hexadecimal status value reported by the device.

Value	Definition
0	Off-line data collection never started.
2	All segments completed without errors.
4	Off-line data collection is suspended by the interrupting command.
5	Off-line data collecting is aborted by the interrupting command.
6	Off-line data collection is aborted with a fatal error.

12.42.2.4 Self-test execution status

Bit	Definition
0-3	Percent Self-test remaining. An approximation of the percent of the self-test routine remaining until completion given in increments of ten percent. Valid values are 0 through 9.
4-7	Current Self-test execution status. **0** The self-test routine completed without error or has never been run. **1** The self-test routine was aborted by the host. **2** The self-test routine was interrupted by the host with a hard or soft reset. **3** The device was unable to complete the self-test routine due to a fatal error or unknown test error. **4** The self-test routine was completed with an unknown element failure. **5** The self-test routine was completed with an electrical element failure. **6** The self-test routine was completed with a servo element failure. **7** The self-test routine was completed with a read element failure. **15** The self-test routine is in progress.

12.42.2.5 Total time in seconds to complete off-line data collection activity

This field tells the host how many seconds the device requires to complete the off-line data collection activity.

12.42.2.6 Off-line data collection capability

Bit	Definition
0	Execute Off-line Immediate implemented bit **0** S.M.A.R.T. Execute Off-line Immediate subcommand is not implemented **1** S.M.A.R.T. Execute Off-line Immediate subcommand is implemented
1	Enable/disable Automatic Off-line implemented bit **0** S.M.A.R.T. Enable/disable Automatic Off-line subcommand is not implemented **1** S.M.A.R.T. Enable/disable Automatic Off-line subcommand is implemented

2 Abort/restart off-line by host bit
- **0** The device will suspend off-line data collection activity after an interrupting command and resume it after a vendor specific event
- **1** The device will abort off-line data collection activity upon receipt of a new command

3 Off-line Read Scanning implemented bit
- **0** The device does not support Off-line Read Scanning
- **1** The device supports Off-line Read Scanning

4 Self-test implemented bit
- **0** Self-test routing is not implemented
- **1** Self-test routine is implemented

5-7 Reserved (0)

12.42.2.7 S.M.A.R.T. Capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the S.M.A.R.T. ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit	Definition
0	Pre-power mode attribute saving capability. If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).
1	Attribute Autosave capability. If bit = 1, the device supports the S.M.A.R.T. ENABLE/ DISABLE ATTRIBUTE AUTOSAVE command.
2-15	Reserved (0)

12.42.2.8 Error logging capability

Bit	Definition
7-1	Reserved (0)
0	The Error Logging support bit. If bit = 1, the device supports the Error Logging

12.42.2.9 Self-test failure check point

This byte indicates the section of self-test where the device detected a failure.

12.42.2.10 Self-test completion time

These bytes are the minimum time in minutes to complete the self-test.

12.42.2.11 Data Structure Checksum

The Data Structure Checksum is the 2's complement of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

12.42.3 Device Attribute Thresholds data structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Thresholds. All multibyte fields shown in these data structures are in byte ordering, that is, that the least significant byte occupies the lowest numbered byte address location in the field.

The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

Table 119: Device Attribute Thresholds Data Structure

Description	Byte	Offset	Value
Data Structure Revision Number	2	00h	0010h
1st Device Attribute	12	02h	
...	..		
30th Device Attribute	12	15Eh	
Reserved	18	16Ah	00h
Vendor specific	131	17Ch	00h
Data structure checksum	1	1FFh	
	512		

12.42.3.1 Data Structure Revision Number

This value is the same as the value used in the Device Attributes Values Data Structure.

12.42.3.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure are in the same order and correspond to the entries in the Individual Attribute Data Structure.

Table 120: Individual Threshold Data Structure

Description	Byte	Offset
Attribute ID Number (01h to FFh)	1	00h
Attribute Threshold	1	01h
Reserved (00h)	10	02h
Total Bytes	12	

12.42.3.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

12.42.3.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable.

12.42.3.5 Data Structure Checksum

The Data Structure Checksum is the two's complement of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

12.42.4 S.M.A.R.T. Log Directory

The following table defines the 512 bytes that make up the S.M.A.R.T. Log Directory. The S.M.A.R.T. Log Directory is S.M.A.R.T. Log Address zero and is defined as one sector long.

Table 121: S.M.A.R.T. Log Directory

Description	Byte	Offset
S.M.A.R.T. Logging Version	2	00h
Number of sectors in the log at log address 1	1	02h
Reserved	1	03h
Number of sectors in the log at log address 2	1	04h
Reserved	1	05h
...	...	...
Number of sectors in the log at log address 255	1	1FEh
Reserved	1	1FFH
	512	

The value of the S.M.A.R.T. Logging Version word shall be 01h. The logs at log addresses 80-9Fh shall each be defined as 16 sectors long.

12.42.5 S.M.A.R.T. summary error log sector

The following figure defines the 512 bytes that make up the SMART summary error log sector. All multibyte fields shown in this data structure follow the ATA/ATAPI-6 specifications for byte ordering.

Table 122: S.M.A.R.T. summary error log sector

Description	Byte	Offset
S.M.A.R.T. error log version	1	00h
Error log pointer	1	01h
1st error log data structure	90	02h
2nd error log data structure	90	5Ch
3rd error log data structure	90	B6h
4th error log data structure	90	110h
5th error log data structure	90	16Ah
Device error count	2	1C4h
Reserved	57	1C6h
Data structure checksum	1	1FFh
	512	

12.42.5.1 S.M.A.R.T. error log version

This value is set to 01h.

12.42.5.2 Error log pointer

This points to the most recent error log data structure. Only values 1 through 5 are valid.

12.42.5.3 Device error count

This field contains the total number of errors. The value will not roll over.

12.42.5.4 Error log data structure

The data format of each error log data structure is shown below.

Table 123: Error log data structure

Description	Byte	Offset
1st command data structure	12	00h
2nd command data structure	12	0Ch
3rd command data structure	12	18h
4th command data structure	12	24h
5th command data structure	12	30h
Error data structure	30	3Ch
	90	

12.42.5.5 Command data structure

Data format of each command data structure is shown below.

Table 124: Command data structure

Description	Byte	Offset
Device Control register	1	00h
Features register	1	01h
Sector count register	1	02h
Sector number register	1	03h
Cylinder Low register	1	04h
Cylinder High register	1	05h
Device/Head register	1	06h
Command register	1	07h
Time stamp (ms from Power On)	4	08h
	12	

12.42.5.6 Error data structure

Data format of error data structure is shown below.

Table 125: Error data structure

Description	Byte	Offset
Reserved	1	00h
Error register	1	01h
Sector count register	1	02h
Sector number register	1	03h
Cylinder Low register	1	04h
Cylinder High register	1	05h
Device/Head register	1	06h
Status register	1	07h
Extended error data (vendor specific)	19	08h
State	1	1Bh
Life time stamp (hours)	2	1Ch
	30	

The state field contains a value indicating the device state when command was issued to the device.

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle
x4h	S.M.A.R.T. Off-line or Self-test
x5h-xAh	Reserved
xBh-xFh	Vendor specific

The value of 'x' is vendor specific

12.42.6 Self-test log data structure

The following table defines the 512 bytes that make up the Self-test log sector. All multibyte fields shown in these data structures follow the ATA/ATAPI-5 specifications for byte ordering.

Table 126: Self-test log data structure

Description	Byte	Offset
Data structure revision	2	00h
Self-test number	1	n*18h+02h
Self-test execution status	1	n*18h+03h
Life time power on hours	2	n*18h+04h
Self-test failure check point	1	n*18h+06h
LBA of first failure	4	n*18h+07h
Vendor specific	15	n*18h+08h
...		
Vendor specific	2	1FAh
Self-test log pointer	1	1FCh
Reserved	2	1FDh
Data structure checksum	1	1FFh
	512	

Note: N is 0 through 20

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors.

After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor.

The self-test log index points to the most recent descriptor. When there is no descriptor, the value is 0. When there are one or more descriptors, the value is 1 through 21.

12.42.7 Error reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

Table 127: S.M.A.R.T. Error Codes

Error condition	Status Register	Error Register
A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the Cylinder High and Cylinder Low registers.	51h	04h
A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A S.M.A.R.T. FUNCTION SET command subcommand other than S.M.A.R.T. ENABLE OPERATIONS was received by the device while the device was in a "S.M.A.R.T. Disabled" state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure	51h	10h or 40h
The device is unable to write to its Attribute Values data structure.	51h	10h or 01h

12.43 Standby (E2h/96h)

Table 128: Standby (E2h/96h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 0 0 1 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Standby command causes the device to enter the Standby Mode immediately and to set the auto power down time-out parameter (standby timer).

When the Standby mode is entered, the drive is spun down but the interface remains active. If the drive is already spun down, the spin down sequence is not executed.

During the Standby mode the drive will respond to commands but there is a delay while waiting for the spindle to reach operating speed.

The automatic power down sequence is enabled and the timer starts counting down when the drive returns to Idle mode

Output parameters to the device

Sector Count Time-out Parameter. If it is 0, the time-out interval (Standby Timer) is NOT disabled. If it is non-zero, the automatic power down sequence is enabled. The time-out interval is shown below.

Value	Time-out
0	Timer disabled
1-240	Value x 5 seconds
241-251	(Value-240) x 30 minutes
252	21 minutes
253	8 hours
254	21 minutes 10 seconds
255	21 minutes 15 seconds

When the automatic power down sequence is enabled, the device will enter the Standby mode automatically if the time-out interval expires with no device access from the host. The time-out interval will be reinitialized if there is a drive access before the time-out interval expires.

12.44 Standby Immediate (E0h/94h)

Table 129: Standby Immediate (E0h/94h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 0 1 1 0 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	V	-	0	-	V

The Standby Immediate command causes the device to enter the Standby mode immediately.

The device is spun down but the interface remains active. If the device is already spun down, the spin down sequence is not executed.

During the Standby mode the device will respond to commands, however there will be a delay while waiting for the spindle to reach operating speed.

The Standby Immediate command will not affect the auto power down time-out parameter.

12.45 Write Buffer (E8h)

Table 130: Write Buffer (E8h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	- - - - - - - -		Sector Count	- - - - - - - -
Sector Number	- - - - - - - -		Sector Number	- - - - - - - -
Cylinder Low	- - - - - - - -		Cylinder Low	- - - - - - - -
Cylinder High	- - - - - - - -		Cylinder High	- - - - - - - -
Device/Head	1 - 1 D - - - -		Device/Head	- - - - - - - -
Command	1 1 1 0 1 0 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	0	0	V	0	0		0	V	0	-	-	0	-	V

The Write Buffer command transfers a sector of data from the host to the sector buffer of the device. The sectors of data are transferred through the Data Register 16 bits at a time.

The Read Buffer and Write Buffer commands are synchronized such that sequential Write Buffer and Read Buffer commands access the same 512 byte within the buffer.

12.46 Write DMA (CAh/CBh)

Table 131: Write DMA (CAh/CBh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	1 1 0 0 1 0 1 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	0	0	V	0	V	0	0		0	V	V	V	-	0	-	V

The Write DMA command transfers one or more sectors of data from the host to the device and then the data is written to the disk media.

The sectors of data are transferred through the Data Register16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, then 256 sectors will be transferred.

Sector Number This indicates the sector number of the first sector to be transferred. (L = 0)In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates number of the first sector to be transferred. (L = 0) In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L= 1)

H This indicates the head number of the first sector to be transferred. (L = 0) In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This indicates the retry bit. This bit is ignored.

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred. The Sector Count will be zero unless an unrecoverable error occurs.

Sector Number This indicates the sector number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low	This indicates the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This indicates the head number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 24–27. (L = 1)

12.47 Write DMA Ext (35h)

Table 132: Write DMA Ext Command (35h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		see below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		- 1 - D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 1 0 1 0 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Write DMA Ext command transfers one or more sectors of data from the host to the device, then the data is written to the disk media.

The sectors of data are transferred through the Data Register 16 bits at a time.

The host initializes a slave-DMA channel prior to issuing the command. Data transfers are qualified by DMARQ and are performed by the slave-DMA channel. The device issues only one interrupt per command to indicate that data transfer has terminated and status is available.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output parameters to the device

Sector Count Current	The number of continuous sectors to be transferred low order, bits (7:0)
Sector Count Previous	The number of continuous sectors to be transferred low order, bits (15:8). If zero is specified in the Sector Count register, 65,536 sectors will be transferred.
Sector Number Current	LBA (7:0)
Sector Number Previous	LBA (31:24)
Cylinder Low Current	LBA (15:8)
Cylinder Low Previous	LBA (39:32)

Cylinder High Current	LBA (23:16)
Cylinder High Previous	LBA (47:40)

Input parameters from the device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

12.48 Write DMA Queued (CAh/CBh)

Table 133: Write DMA Queued Command CAh/CBh)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	V V V V V V V V		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	1 1 0 0 1 1 0 0		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

This command executes in a similar manner to a WRITE DMA command. The device may perform a bus release or it may execute the data transfer without performing a bus release if the data is ready to be transferred.

If the device performs a bus release, the host shall reselect the device using the SERVICE command.

When the data transfer has begun, the device does not perform a bus release until the entire data transfer has been completed.

Output parameters to the device

Feature The number of sectors to be transferred low order. A value of 00h indicates that 256 sectors are to be transferred.

Sector Count Bits 7-3 (Tag) contain the Tag for the command being delivered.

Sector Number Starting sector number or LBA address bits 7-0.

Cylinder High/Low Starting cylinder number or LBA address bits 23-:8.

H Starting head number or LBA address bits 27-24.

Input parameters from the device on bus release

Sector Count Bits 7 - 3 (Tag) contain the Tag of the command being bus released.
Bit 2 (REL) is set to one.
Bit 1 (I/O) is cleared to zero.
Bit 0 (C/D) is cleared to zero.

Sector Number, Cylinder High/Low, H n/a.

SRV Cleared to zero when the device performs a bus release. This bit is set to 1 when the device is ready to transfer data.

Input parameters from the device on command complete

Sector Count	Bits 7 - 3 (Tag) contain the Tag of the completed command. Bit 2 (REL) is cleared to zero. Bit 1 (I/O) is set to one. Bit 0 (C/D) is set to one.
Sector Number, Cylinder High/Low, H	Sector address of unrecoverable error (applicable only when an unrecoverable error has occurred).
SRV	Cleared to 0.

12.49 Write DMA Queued Ext (36h)

Table 134: Write DMA Queued Ext Command (36h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	V V V V V V V V		Error		see below
	Previous	V V V V V V V V				
Sector Count	Current	V V V V - - - -		Sector Count	HOB=0	V V V V V V V V
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		- 1 - D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 1 0 1 1 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
V	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

This command executes in a similar manner to a WRITE DMA EXT command. The device may perform a bus release or may execute the data transfer without performing a bus release if the data is ready to transfer.

If the device performs a bus release, the host shall re-select the device using the SERVICE command.

Once the data transfer is begun, the device shall not perform a bus release until the entire data transfer has been completed.

Output parameters to the device

Feature Current The number of continuous sectors to be transferred low order, bits (7:0)

Feature Previous The number of continuous sectors to be transferred low order, bits (15:8). A value of 0000h in the Feature register indicates that 65,536 sectors are to be transferred.

Sector Count Current Bits 7 - 3 (Tag) contain the Tag for the command being delivered.

Sector Number Current LBA (7:0)

Sector Number Previous LBA (31:24)

Cylinder Low Current LBA (15:8)

Cylinder Low Previous LBA (39:32)

Cylinder High Current LBA (23:16)

Cylinder High Previous LBA (47:40)

Input parameters from the device on Bus Release

Sector Count	Bits 7 - 3 (Tag) contain the Tag of the command being bus released. Bit 2 (REL) is set to one. Bit 1 (I/O) is cleared to zero. Bit 0 (C/D) is cleared to zero.

Sector Number, Cylinder High/Low, H n/a.

SRV	Cleared to zero when the device performs a bus release. This bit is set to 1 when the device is ready to transfer data.

Input parameters from the device on Command Complete

Sector Count (HOB-0)	Bits 7 - 3 (Tag) contain the Tag of the command being bus released. Bit 2 (REL) is cleared to one. Bit 1 (I/O) is set to zero. Bit 0 (C/D) is set to zero.
Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error (applicable only when an unrecoverable error has occurred).
SRV	Cleared to zero.

12.50 Write Log Ext (3Fh)

Table 135: Write Log Ext Command (3Fh)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		See below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Cylinder High	Current	- - - - - - - -		Cylinder High	HOB=0	- - - - - - - -
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Device/Head		- 1 - D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 1 1 1 1 1		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	V	0	V	0	V	0	V		0	V	0	V	-	0	-	V

This command writes a specified number of 512 byte data sectors to the specific log. The device shall interrupt for each DRQ block transferred.

Output parameters to the device

Sector Count Current The number of sectors to be written to the specified log low order, bits (7:0).

Sector Count Previous The number of sectors to be written to the specified log high orders, bits (15:8). If the number of sectors is greater than the number indicated in the Log directory, which is available in Log number zero, the device shall return command aborted. The log transferred to the device shall be stored by the device starting at the first sector in the specified log.

Sector Number Current The log to be written as described in Table 79: “Log Address Definition” on page 141. If the host attempts to write to a read only log address, the device shall return command aborted.

Cylinder Low Current The first sector of the log to be written low order, bits (7:0).

Cylinder Low Previous The first sector of the log to be written high order, bits (15:8).

If the feature set associated with the log specified in the Sector Number register is not supported or enabled, or if the values in the Sector Count, Sector Number or Cylinder Low registers are invalid, the device shall return command aborted. If the host attempts to write to a read only log address, the device shall return command aborted.

12.51 Write Long (32h/33h)

Table 136: Write Long (32h/33h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	0 0 0 0 0 0 0 1		Sector Count	- - - - - - - V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 0 1 1 0 0 1 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Write Long command transfers the data and the ECC bytes of the designated one sector from the host to the device, then the data and the ECC bytes are written to the disk media.

After 512 bytes of data have been transferred, the device will keep setting DRQ = 1 to indicate that the device is ready to receive the ECC bytes from the host. The data is transferred 16 bits at a time and the ECC bytes are transferred 8 bits at a time. The number of ECC bytes are either 4 or 40 according to setting of the Set Feature option. The default number after power on is 4 bytes.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. The Sector Count must be set to one.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High) (L = 1)

H This indicates the head number of the sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 24–27. (L = 1)

R The retry bit. This bit is ignored.

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred.

Sector Number This indicates the sector number of the sector to be transferred. (L = 0)
In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low	This indicates the cylinder number of the sector to be transferred. (L = 0) In LBA mode this register contains current the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This indicates the head number of the sector to be transferred. (L = 0) In LBA mode this register contains current the LBA bits 24–27. (L = 1)

The drive internally uses 52 bytes of ECC on all data read or writes. The 4-byte mode of operation is provided by means of an emulation technique. As a consequence of this emulation it is recommended that 52-byte ECC mode be used for all tests to confirm the operation of the ECC hardware of the drive. Unexpected results may occur if such testing is performed using 4-byte mode.

12.52 Write Multiple (C5h)

Table 137: Write Multiple (C5h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	1 1 0 0 0 1 0 1		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	V	V	-	0	-	V

The Write Multiple command transfers one or more sectors from the host to the device. The data is then written to the disk media.

Command execution is identical to the Write Sectors command except that an interrupt is generated for each block as defined by the Set Multiple command instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If the Sector Count of zero is specified, 256 sectors will be transferred.

Sector Number This indicates the sector number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 24–27. (L = 1)

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred. The Sector Count will be zero, unless an unrecoverable error occurs.

Sector Number This indicates the sector number of the last transferred sector. (L = 0)
In LBA mode this register contains current the LBA bits 0–7. (L = 1)

Cylinder High/Low	This indicates the cylinder number of the last transferred sector. (L = 0) In LBA mode this register contains the current LBA bits 8–15 (Low) and bits 16–23 (High). (L = 1)
H	This indicates the head number of the last transferred sector. (L = 0) In LBA mode this register contains current the LBA bits 24–27. (L = 1)

12.53 Write Multiple Ext (39h)

Table 138: Write Log Ext Command (3Fh)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	V V V V V V V V		Error		See below
	Previous	V V V V V V V V				
Sector Count	Current	V V V V V - - -		Sector Count	HOB=0	V V V V V V V V
	Previous	- - - - - - - -			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		- 1 - D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 1 0 1 1 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	V	V	-	0	-	V

The Write Multiple Ext command transfers one or more sectors from the host to the device, then the data is written to the disk media.

Command execution is identical to the Write Sector(s) Ext command except that an interrupt is generated for each block (as defined by the Set Multiple command) instead of for each sector. The sectors are transferred through the Data Register 16 bits at a time.

Output parameters to the device

Sector Count Current The number of continuous sectors to be transferred low order, bits (7:0)

Sector Count Previous The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified in the Sector Count register, then 65,536 sectors shall be transferred.

Sector Number Current LBA (7:0)

Sector Number Previous LBA (31:24)

Cylinder Low Current LBA (15:8)

Cylinder Low Previous LBA (39:32)

Cylinder High Current LBA (23:16)

Cylinder High Previous LBA (47:40)

Input parameters from the device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

12.54 Write Sectors (30h/31h)

Table 139: Write Sectors command (30h/31h)

Command Block Output Registers			Command Block Input Registers	
Register	7 6 5 4 3 2 1 0		Register	7 6 5 4 3 2 1 0
Data	- - - - - - - -		Data	- - - - - - - -
Feature	- - - - - - - -		Error	see below
Sector Count	V V V V V V V V		Sector Count	V V V V V V V V
Sector Number	V V V V V V V V		Sector Number	V V V V V V V V
Cylinder Low	V V V V V V V V		Cylinder Low	V V V V V V V V
Cylinder High	V V V V V V V V		Cylinder High	V V V V V V V V
Device/Head	1 L 1 D H H H H		Device/Head	- - - - H H H H
Command	0 0 1 1 0 0 0 R		Status	see below

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	0	V	-	0	-	V

The Write Sectors command transfers one or more sectors from the host to the device. The data is then written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output parameters to the device

Sector Count This indicates the number of continuous sectors to be transferred. If zero is specified, 256 sectors will be transferred.

Sector Number This indicates the sector number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 8–15 (Low) and bits 16–23 (High) (L = 1)

H This indicates the head number of the first sector to be transferred. (L = 0)
In LBA mode this register contains the LBA bits 24–27. (L = 1)

R This indicates the retry bit. this bit is ignored.

Input parameters from the device

Sector Count This indicates the number of requested sectors not transferred. This will be zero unless an unrecoverable error occurs.

Sector Number This indicates the sector number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 0–7. (L = 1)

Cylinder High/Low This indicates the cylinder number of the last transferred sector. (L = 0)

In LBA mode this register contains the current LBA bits 8–15 (Low) and 16–23 (High). (L = 1)

H This indicates the head number of the last transferred sector. (L = 0)
In LBA mode this register contains the current LBA bits 24–27. (L = 1)

12.55 Write Sector(s) (34h)

Table 140: Write Sector(s) Command (34h)

Command Block Output Registers				Command Block Input Registers		
Register		7 6 5 4 3 2 1 0		Register		7 6 5 4 3 2 1 0
Data Low		- - - - - - - -		Data Low		- - - - - - - -
Data High		- - - - - - - -		Data High		- - - - - - - -
Feature	Current	- - - - - - - -		Error		See below
	Previous	- - - - - - - -				
Sector Count	Current	V V V V V V V V		Sector Count	HOB=0	- - - - - - - -
	Previous	V V V V V V V V			HOB=1	- - - - - - - -
Sector Number	Current	V V V V V V V V		Sector Number	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder Low	Current	V V V V V V V V		Cylinder Low	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Cylinder High	Current	V V V V V V V V		Cylinder High	HOB=0	V V V V V V V V
	Previous	V V V V V V V V			HOB=1	V V V V V V V V
Device/Head		- 1 - D - - - -		Device/Head		- - - - - - - -
Command		0 0 1 1 0 1 0 0		Status		See below ...

Error Register									Status Register							
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0
CRC	UNC	0	IDN	0	ABT	T0N	AMN		BSY	RDY	DF	DSC	DRQ	COR	IDX	ERR
0	0	0	V	0	V	0	0		0	V	V	V	-	0	-	V

The Write Sectors command transfers one or more sectors from the host to the device; the data is then written to the disk media.

The sectors are transferred through the Data Register 16 bits at a time.

If an uncorrectable error occurs, the write will be terminated at the failing sector.

Output parameters to the device

Sector Count Current The number of continuous sectors to be transferred low order, bits (7:0)

Sector Count Previous The number of continuous sectors to be transferred high order, bits (15:8). If zero is specified, 65,536 sectors shall be transferred.

Sector Number Current LBA (7:0)

Sector Number Previous LBA (31:24)

Cylinder Low Current LBA (15:8)

Cylinder Low Previous LBA (39:32)

Cylinder High Current LBA (23:16)

Cylinder High Previous LBA (47:40)

Input parameters from the device

Sector Number (HOB=0)	LBA (7:0) of the address of the first unrecoverable error.
Sector Number (HOB=1)	LBA (31:24) of the address of the first unrecoverable error.
Cylinder Low (HOB=0)	LBA (15:8) of the address of the first unrecoverable error.
Cylinder Low (HOB=1)	LBA (39:32) of the address of the first unrecoverable error.
Cylinder High (HOB=0)	LBA (23:16) of the address of the first unrecoverable error.
Cylinder High (HOB=1)	LBA (47:40) of the address of the first unrecoverable error.

13.0 Time-out values

The timing of BSY and DRQ in Status Register are shown in the table below.

Table 141: Time-out values

	INTERVAL	START	STOP	TIME-OUT
Power On	Device Busy After Power On	Power On	Status Register BSY=1	400 ns
	Device Ready After Power On	Power On	Status Register BSY=1 and RDY=1	31 sec
Software Reset	Device Busy After Software Reset	Device Control Register RST=1	Status Register BSY=1	400 ns
	Device Ready After Software Reset	Device Control Register RST=0 After RST=1	Status Register BSY=0 and RDY=1	31 sec
Hard Reset	Device Busy After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=1	400 ns
	Device Ready After Hard Reset	Bus RESET Signal Asserted	Status Register BSY=0 and RDY=1	31 sec
Data In Command	Device Busy After Command Code Out	OUT To Command Register	Status Register BSY=1	400 ns
	Interrupt, DRQ For Data Transfer In	Status Register BSY=1	Status Register BSY=0 and DRQ=1, Interrupt	30 sec
	Device Busy After Data Transfer In	256th Read From Data Register	Status Register BSY=1	10 μs
Data Out Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Device Busy After Data Transfer Out	256th Write From Data Register	Status Register BSY=1	5 μs
	Interrupt For Data Transfer Out	Status Register BSY=1	Status Register BSY=0 and RDY=1 Interrupt	30 sec
Non-Data Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns
	Interrupt For Command Complete	Status Register BSY=1	Interrupt	30 sec
DMA Data Transfer Command	Device Busy After Command Code Out	OUT to Command Register	Status Register BSY=1	400 ns

Command category is referred to in section 11.0, "Command protocol" on page 99.

The abbreviations "ns", "μs", "ms," and "sec" mean nanoseconds, microseconds, milliseconds, and seconds, respectively.

If the host detects a time-out while waiting for a response from the device, we recommend that the host system execute a Soft reset and then retry the command.

.

Index

48-bit Address Feature 97

A

Abbreviations 1
Acoustics 39
Actuator 9
Address Offset 95
Advanced Power Managemen 93
Automatic Acoustic Management 94

B

BSMI mark 41

C

Cable noise interference 32
Cabling 60
Capacity, formatted 11
Caution 3
CE mark 41
Command descriptions 105
Command overhead 15
Command protocol 99
Command table 86
Connector locations 35
Control electronics 9
Corrosion test 29
CSA approval 40
C-TICK mark 41
Cylinder allocation 13

D

Data In commands 99
Data Out Commands 100
Data Reliability 32
Data sheet 11, 12
DC power connector 43
DC power requirements 29
Defect flagging strategy 21
Deviations from standard 63

DMA commands 103
DMA Data Transfer commands 103
Drive characteristics 11
Drive format 13
Drive ready time 17

E

Electrical interface 43
Electromagnetic compatibility 40, 41
Environment 28

F

Fixed-disk subsystem 9
Flammability 40
Flush Cache 115
Formatted capacity 11
Functional specification 7

G

General 1
General features 5

H

Head disk assembly 9
Head disk assembly data 9
Heads unload 35
Humidity 28

I

Identification labels 39
Input voltage 29
Interface logic signal levels 48
Interface specification 61

J

Jumper pin location 23
Jumper positions 24
Jumper settings 23

L

Labels, Identification 39
Latency, average 17
Load/unload 32

M

Mechanical specifications 33
Mode transition time 20
Mounting hole locations 34
Mounting orientation 35

N

Non-data commands 102

O

Operating modes 20
description 18
Operating shock 37

P

Packaging 41
Passwords 83
Performance characteristics 15
Physical dimensions 33
PIO timings 49
Power consumption effiency 31
Power management features 78
Power supply current 29
Preventive maintenance 32
Protected Area 87

R

Reassign function 91
References 1
Register set 65
Registers 65
Reset timings 48

S

S.M.A.R.T. Function Set 186
Safety 40
Secondary circuit protection 40
Sector Addressing 76
Security Mode Feature Set 82
Shock 36
Signal definitions 44
Specification 23

T

Temperature 28
Time-out values 221

U

UL approval 40

V

Vibration 36

W

Weight 33
Write Buffer 201

Hitachi Global Storage Technologies
5600 Cottle Road
San Jose, CA 95193
Produced in the United States

09/2005

21 September 2005